AMENDMENT

Am186™ESLV and Am188™ESLV

High-Performance, 80L186- and 80L188-Compatible, Low-Voltage, 16-Bit Embedded Microcontrollers

Advanced Micro Devices

Except as noted in this amendment, the Am186ES and Am188ES microcontrollers data sheet, order# 20002, contains the detailed specifications for the Am186ESLV and Am188ESLV microcontrollers.

DISTINCTIVE CHARACTERISTICS

- **E86™ family 80L186- and 80L188-compatible microcontrollers with enhanced bus interface**
  - — Lower system cost with higher performance
  - — 3.3-V ±0.3-V operation
- **High performance**
  - — 20-MHz and 25-MHz operating frequencies
  - — Supports zero-wait-state operation at 25 MHz with 110-ns static memory
  - — 1-Mbyte memory address space
  - — 64-Kbyte I/O space
- **Enhanced features provide improved memory access and eliminate the need for a 2x clock input**
  - — Non-multiplexed address bus
  - — Processor operates at the clock input frequency
  - — On the Am186™ESLV microcontroller, 8-bit or 16-bit memory and I/O static bus option
- **Enhanced integrated peripherals provide increased functionality, while reducing system cost**
  - — Thirty-two programmable I/O (PIO) pins
  - — Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers
  - — Serial port hardware handshaking with $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{ENRX}}$, and $\overline{\text{RTR}}$ selectable for each port
  - — Multidrop 9-bit serial port protocol
  - — Independent serial port baud rate generators
  - — DMA to and from the serial ports
  - — Watchdog timer can generate NMI or reset
  - — A pulse-width demodulation option
  - — A data strobe, true asynchronous bus interface option included for $\overline{\text{DEN}}$
  - — Pseudo static RAM (PSRAM) controller includes auto refresh capability
  - — Reset configuration register
- **Familiar 80L186 peripherals**
  - — Two independent DMA channels
  - — Programmable interrupt controller with up to eight external and eight internal interrupts
  - — Three programmable 16-bit timers
  - — Programmable memory and peripheral chip-select logic
  - — Programmable wait state generator
  - — Power-save clock divider
- **Software-compatible with the 80L186/188 microcontrollers with widely available native development tools**
- **Available in the following packages:**
  - — 100-pin, thin quad flat pack (TQFP)
  - — 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186™ESLV and Am188™ESLV microcontrollers are the ideal upgrade for 80L186/188 designs requiring low-power operation, 80L186/188 compatibility, increased performance, serial communications, and a direct bus interface.

The Am186ESLV and Am188ESLV microcontrollers integrate the functions of the CPU, non-multiplexed address bus, three timers, a watchdog timer, chip selects, interrupt controller, two DMA controllers, PSRAM controller, asynchronous serial ports, programmable bus sizing, and programmable I/O pins on one chip. Compared to the 80L186/188 microcontrollers, the Am186ESLV and Am188ESLV controllers can reduce the size, power consumption, and cost of embedded systems, while increasing reliability and performance.

The Am186ESLV and Am188ESLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the mass storage, communications, and general embedded markets. Specific applications include disk drives, desktop terminals, hand-held terminals, fax machines, printers, photocopiers, feature phones, cellular phones, PBXs, multiplexers, and industrial controls.

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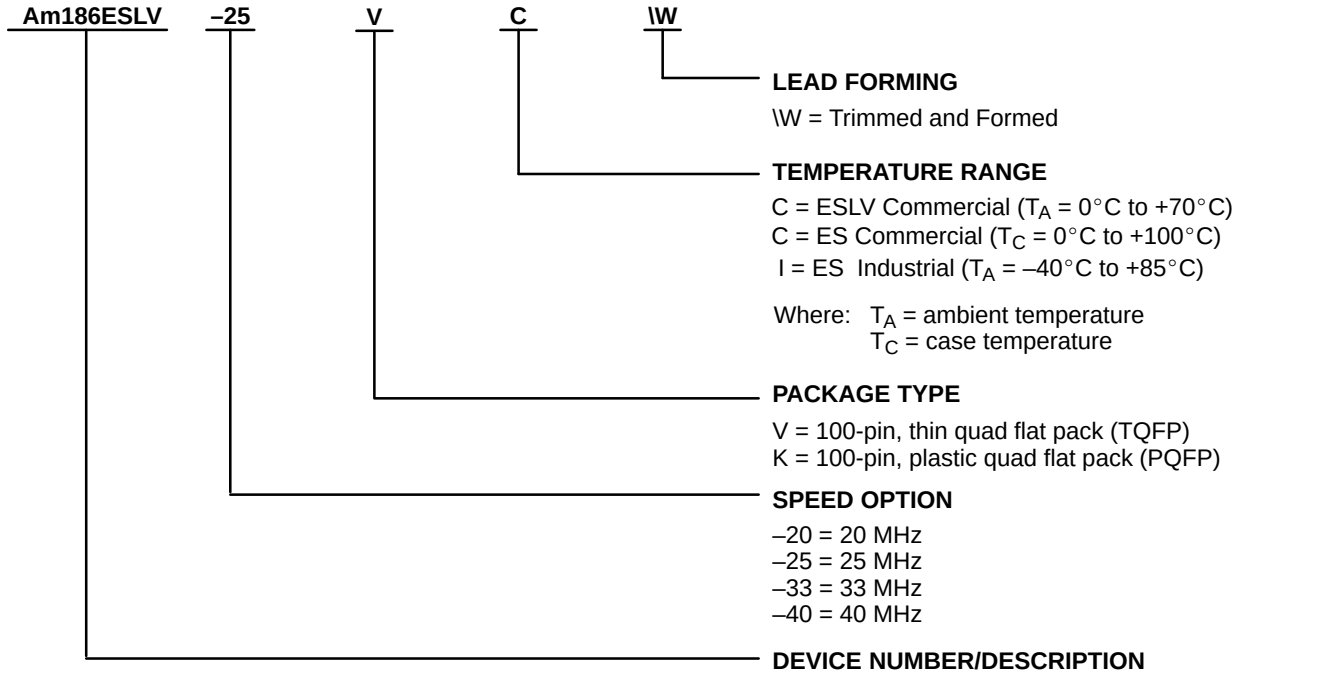
Issue Date: April **1996**

ORDERING INFORMATION

Standard Products

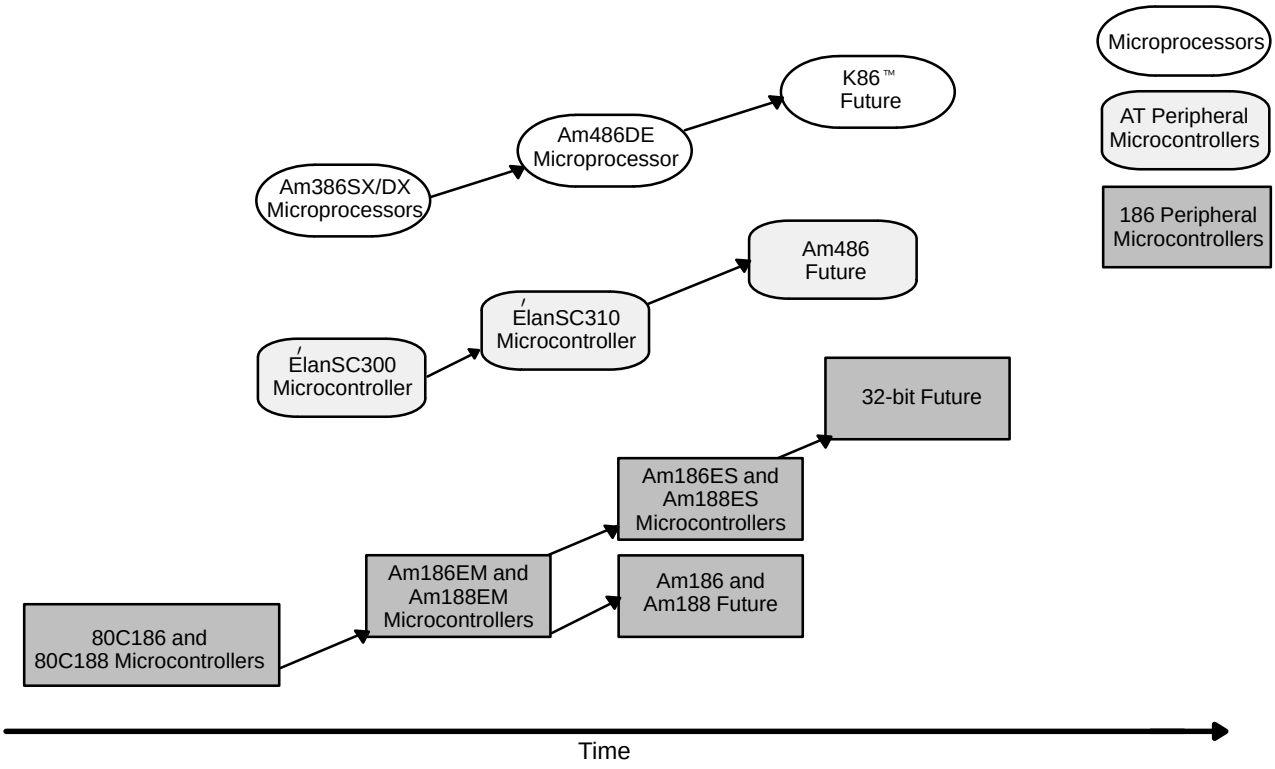
AMD® standard products are available in several packages and operating ranges. The order numbers (valid combinations) are formed by a combination of the elements below.



Valid Combinations	
Am186ESLV–20 Am186ESLV–25	VC\W or KC\W
Am188ESLV–20 Am188ESLV–25	VC\W or KC\W
Am186ES–20 Am186ES–25 Am186ES–33 Am186ES–40	VC\W or KC\W
Am188ES–20 Am188ES–25 Am188ES–33 Am188ES–40	VC\W or KC\W
Am186ES–20 Am186ES–25	KI\W
Am188ES–20 Am188ES–25	KI\W

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.



The E86 Family of Embedded Microprocessors and Microcontrollers

RELATED AMD PRODUCTS

E86 Family Devices

Device	Description
80C186	16-bit microcontroller
80C188	16-bit microcontroller with 8-bit external data bus
80L186	Low-voltage, 16-bit microcontroller
80L188	Low-voltage, 16-bit microcontroller with 8-bit external data bus
Am186EM	High-performance, 80C186-compatible, 16-bit embedded microcontroller
Am188EM	High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus
Am186EMLV	High-performance, 80L186-compatible, low-voltage, 16-bit embedded microcontroller
Am188EMLV	High-performance, 80L188-compatible, low-voltage, 16-bit embedded microcontroller with 8-bit external data bus
Am186ES	High-performance, 80C186-compatible, 16-bit embedded microcontroller
Am188ES	High-performance, 80C188-compatible, 16-bit embedded microcontroller with 8-bit external data bus
Élan™ SC300	Highly integrated, low-power, 32-bit microcontroller
Élan™ SC310	Highly integrated, single-chip, 32-bit, PC/AT microcontroller
Am386®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
Am386®SX	High-performance, 32-bit embedded microprocessor with 16-bit external data bus
Am486®DE	High-performance, 32-bit embedded microprocessor with 32-bit external data bus

KEY FEATURES AND BENEFITS

The Am186ESLV and Am188ESLV microcontrollers extend the AMD family of microcontrollers based on the industry-standard x86 architecture. The Am186ESLV and Am188ESLV microcontrollers are higher-performance, more-integrated versions of the 80L186/188 microprocessors. Upgrading to the Am186ESLV and Am188ESLV microcontrollers is an attractive solution for several reasons:

- **Low voltage**—Reduces power consumption.
- **Minimized total system cost**—New peripherals and on-chip system interface logic on the Am186ESLV and Am188ESLV microcontrollers reduce the cost of existing 80L186/188 designs.
- **x86 software compatibility**—80L186/188 compatible and upward compatible with the other members of the AMD E86 family.
- **Enhanced performance**—The Am186ESLV and Am188ESLV microcontrollers increase the performance of 80L186/188 systems, and the non-multiplexed address bus offers faster, unbuffered access to memory.
- **Enhanced functionality**—The new and enhanced on-chip peripherals of the Am186ESLV and Am188ESLV microcontrollers include two asynchronous serial ports, 32 PIOs, a watchdog timer, additional interrupt pins, a pulse-width demodulation option, DMA directly to and from the serial ports, 8-bit and 16-bit static bus sizing, a PSRAM controller, a 16-bit reset configuration register, and enhanced chip-select functionality.

Application Considerations

The integration enhancements of the Am186ESLV and Am188ESLV microcontrollers provide a high-performance, low-cost solution for 16-bit embedded microcontroller designs. The non-multiplexed address bus eliminates the need for system support logic to interface memory devices, while the multiplexed address/data bus maintains the value of previously engineered, customer-specific peripherals and circuits within the upgraded design.

Clock Generation

The integrated clock generation circuitry of the Am186ESLV and Am188ESLV microcontrollers allows the use of a times-one crystal frequency. The design in Figure 1 achieves 25-MHz CPU operation, while using a 25-MHz crystal.

Memory Interface

The integrated memory controller logic of the Am186ESLV and Am188ESLV microcontrollers provides a direct address bus interface to memory devices. An external address latch controlled by the address latch enable (ALE) signal is no longer needed. Individual byte-write-enable signals are provided to eliminate the need for external high/low byte-write-enable circuitry. The maximum programmable bank size for the memory chip-select signals has been increased to facilitate the use of high-density memory devices.

The improved memory timing specifications for the Am186ESLV and Am188ESLV microcontrollers allow zero-wait-state operation with 110-ns memory access times at 25-MHz CPU clock speed. This reduces overall system cost significantly by allowing the use of a more commonly available memory speed and technology.

Direct Memory Interface Example

Figure 1 illustrates the Am186ESLV microcontroller direct memory interface. The processor A19–A0 bus connects to the memory address inputs, the AD bus connects to the data inputs and outputs, and the chip selects connect to the memory chip-select inputs.

The $\overline{RD}$ output connects to the SRAM Output Enable ($\overline{OE}$) pin for read operations. Write operations use the byte write enables connected to the SRAM Write Enable ($\overline{WE}$) pins.

The example design uses 2-Mbit memory technology (256 Kbytes) to fully populate the available address space. Two flash PROM devices provide 512 Kbytes of nonvolatile program storage, and two static RAM devices provide 512 Kbytes of data storage area.

Figure 1 also shows an implementation of an RS-232 console or modem communications port. The RS-232-to-CMOS voltage-level converter is required for the electrical interface with the external device.

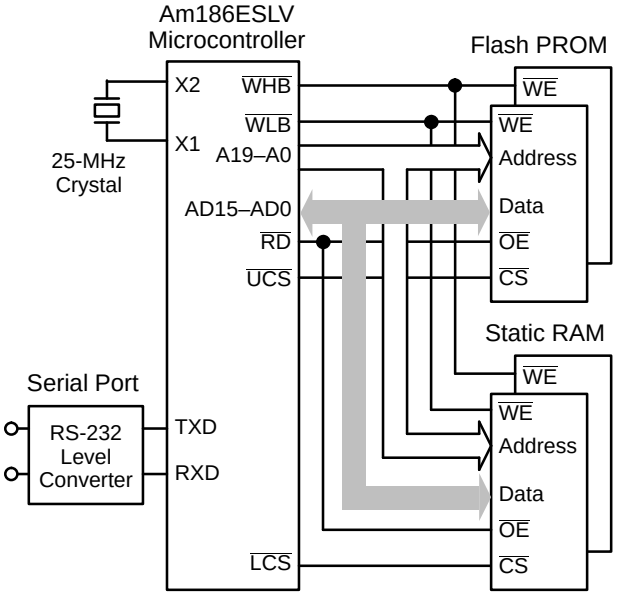


Figure 1. Example System Design

Am186ESLV and Am188ESLV ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias:

Commercial (T_A) . . . . . 0°C to +70°C

Storage temperature . . . . . –65°C to +150°C

Voltage on any pin with respect to ground . . . . . –1.0 V to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

T_A . . . . . 0°C to + 70°C

V_{CC} up to 25 MHz . . . . . 3.3 V ± 0.3 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage (Except X1)		– 0.5	0.6	V
V_{IL1}	Clock Input Low Voltage (X1)		– 0.5	0.8	V
V_{IH}	Input High Voltage (Except $\overline{RES}$ and X1)		2.0	V_{CC} + .5	V
V_{IH1}	Input High Voltage ($\overline{RES}$)		2.4	V_{CC} + .5	V
V_{IH2}	Clock Input High Voltage (X1)		V_{CC} – 0.8	V_{CC} + .5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL} = 1.0 mA (others)		0.45	V
V_{OH}	Output High Voltage[a]	I_{OH} = –100 µA @ V_{CC} – 0.5	V_{CC} – 0.5	V_{CC}	V
I_{CC}	Power Supply Current @ 0°C	V_{CC} = 3.6 V [b]		2.75	mA/ MHz
I_{LI}	Input Leakage Current @ 0.5 MHz	0.45 V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current @ 0.5 MHz	0.45 V ≤ V_{OUT} ≤ V_{CC}[c]		±10	µA

Notes:

a The $\overline{LCS}$/$\overline{ONCE}$0, $\overline{MCS}$3–$\overline{MCS}$0, $\overline{UCS}$/$\overline{ONCE}$1, *and* $\overline{RD}$ *pins have weak internal pullup resistors. Loading the* $\overline{LCS}$/$\overline{ONCE}$0 *and* $\overline{UCS}$/$\overline{ONCE}$1 *pins in excess of* I_{OH} *= –100* µA *during reset can cause the device to go into the ONCE mode of operation.*

b Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open but held High or Low.

c Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Clock (20 MHZ and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
CLKOUT Timing							
70	t_{CICOB}	X1 to CLKOUTB Skew		TBD		TBD	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L *= 50 pF. For switching tests,* V_{IL} *= 0.45 V and* V_{IH} *= 2.4 V, except at X1 where* V_{IH} *=* V_{CC} *– 0.5 V.*

Capacitance

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	@ 1 MHz		10	pF
C_{IO}	Output or I/O Capacitance	@ 1 MHz		20	pF

Note:

Capacitance limits are guaranteed by characterization.

Power Supply Current

For the typical system specification shown in Figure 2, I_{CC} has been measured at 4.0 mA per MHz of system clock. The typical system is measured while the system is executing code in a representative application with maximum voltage and maximum case temperature. Actual power supply current is dependent on system design and may be greater or less than the typical I_{CC} figure presented here.

Typical current in Figure 2 is given by:

$$I_{CC} = 4.0\ mA \cdot freq\ (MHz)$$

Please note that dynamic I_{CC} measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs.

For this I_{CC} measurement, the device was set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 35 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh and DMA are enabled
- PLL in bypass mode

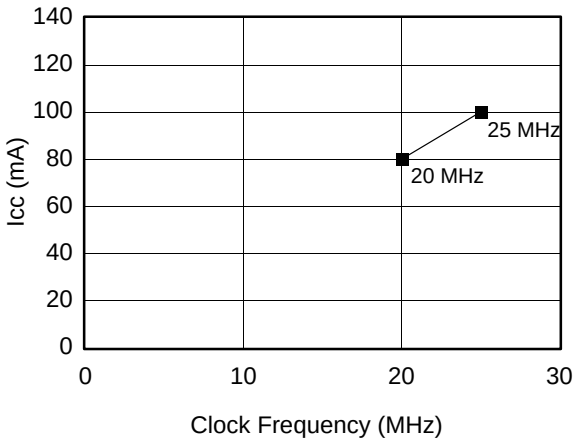


Figure 2. Typical I_{CC} Versus Frequency

Table 1 shows the variables that are used to calculate the typical power consumption value for each version of the Am186ESLV and Am188ESLV microcontrollers.

Table 1. Typical Power Consumption Calculation

MHz · I_{CC} · Volts / 1000 = P			Typical Power (P) in Watts
MHz	Typical I_{CC}	Volts	
20	4.0	3.6	0.288
25	4.0	3.6	0.360