Applied Microsystems
CORPORATION

SuperTAP™ Advanced Development Tool for AMD® Architectures

For Am186/188™ ED, EM, EMLV, ER, ES, ESLV

Compact and feature-rich, SuperTAP is the best development tool in the industry.

HIGHLIGHTS

- Industry's most portable, and versatile in-circuit tool:
  - Software development and test
  - Hardware design and debug
  - Integration
  - Manufacturing Test
  - Field Service
- For software development, SuperTAP is better than a monitor or ROM Emulator:
  - Provides communications path between target and host debugger *without* using target resources
  - Provides run control over the execution of code
  - Provides fast code downloads
  - Provides read/write access to registers and memory
  - Provides both hardware and software breakpoints
  - Real-time view and control of code execution history
  - Visibility of events (bus cycle and code conditions)
  - Ability to map memory address space
  - Works on stable or unstable systems
  - Ability to revive system after software crash
  - Extensive macro language automates debugging
  - Integrated, interactive RTOS kernel support
  - Null target mode allows code development without a target system
- For hardware design and integration, SuperTAP's advanced emulator features fit in a hand-held package:
  - Real-Time emulation to 40 MHz
  - Internal auto-select 3-volt or 5-volt processor support
  - Selectable 8- and 16-bit bus support
  - 64K frame trace buffer with timestamp
  - Trace pre-qualification, positioning and post-filtering
  - Advanced, GUI State-Machine Event System
  - Non-Stop Emulation (NSE™) Trace and Event Systems
  - Overlay Memory substitution for RAM and ROM
  - Versatile communications include 115KBaud RS232, High-Speed RS422
  - Pin-Tracking Management System for Am186 family
  - Complete Am186 PQFP and TQFP adapter support

SuperTAP™—Price and Performance

In the tradition of CodeTAP®, SuperTAP was designed with advanced technology to give embedded engineers all the debugging functions they use most, such as software and hardware breakpoints and modification of memory and processor registers.

As Applied's third generation CodeTAP, SuperTAP sets a new standard in emulation, adding high-performance features such as a real-time 64K deep trace buffer (including address, data, processor status, and timestamp) target monitoring, selectable triggering, extended overlay memory and communications—all in an affordable, small-footprint device.

With support for popular compilers, real-time operating systems and hosts, SuperTAP fits easily into your environment. And thanks to its low cost, you can increase tool availability, boost the whole team's productivity, and reduce time to market.

Patented Emulation Technology

Applied invented CodeTAP emulation technology (U.S. patent No. 5,228,039) to provide low-cost visibility and control for executing and debugging code.

In the CodeTAP tradition, SuperTAP fits in your pocket and is affordable. However, SuperTAP's extended features compare to traditional high-end ICEs and will appeal to software and hardware developers alike.

Behind the tool is a dual processor architecture that guarantees real-time operation, provides fast code downloads and trace uploads. You get the benefit of advanced technology you won't find in look-alike devices.

The bottom line? We think you'll agree—SuperTAP is the best tool in the industry for Am186 debugging.

More Than a Development Tool

SuperTAP offers value that goes beyond the development and debug phases. A complete C macro language lets you automate complex test scripts. Its portable size and communications make SuperTAP quick and easy to use in the field as well as around the office. Clip-on adapters make production line testing go more quickly. And Performance Analysis, including Applied's unique CodeTEST™ product, provides unsurpassed embedded software testing capabilities.

Non-Stop Emulation (NSE™)

SuperTAP was designed to support real-time critical applications. SuperTAP offers NSE trace and event subsystems that can be utilized with the target running or paused. SuperTAP also features fast peek/poke to memory and registers.

NSE™ Trace Subsystem

A 64K deep x 80-bit wide real-time trace buffer helps you locate bugs by providing a history of microprocessor events. On each bus cycle, SuperTAP captures everything you need to track data movement and program execution flow. Captured information includes address, data, processor status, and timestamp.

SuperTAP's NSE (Non-Stop Emulation) feature means you can upload, view and trigger trace without stopping the target processor. Executed code is displayed in assembly and C-source with symbols or raw bus cycles. The trace buffer includes the capability to search for bus cycles containing any combination of address, data, and processor status information to speed analysis.

Triggering trace is easy and SuperTAP offers pre-, post- and center triggering capabilities. Trace information can be pre-qualified through SuperTAP's Event Subsystem, so you capture only the information you want to see. You can also use built-in Logic State Analysis, which tracks external signals, to qualify events. Timestamp provides accurate event timing from 25 ns to 8 hours.

Pin Tracking

SuperTAP's pin tracking management system helps you work with AMD's multiplexed architecture by eliminating I/O pin restrictions.

Unlike other emulators, SuperTAP lets you take advantage of all P10 pins, which is important if you use:

- Pins A17, A18, or A19 as I/O instead of address
- The DMA controller
- The Am186ES programmable 8-bit bus
- Am186ER internal memory

All SuperTAP features, such as the trace, event, and overlay systems, all operate regardless of which pins are used for I/O, even address pins.

Breakpoint Subsystem

Extensive breakpoints work together with the Event System to facilitate code and hardware testing and analysis. You can set breakpoints in your source code symbolically, by specifying function or variable names, or you can just point and click.

You can detect a variety of events using software breakpoints, hardware access breakpoints, and hardware execution breakpoints. Hardware execution breakpoints break immediately before an instruction executes. They prevent false triggering due to pre-fetching. Unlike software breakpoints, hardware execution breakpoints work in ROM as well as RAM.

Hardware access breakpoints can trigger on address, data value, and cycle type. Cycle types include read, write, I/O, DMA, interrupt-acknowledge, and pre-fetch.

NSE™ Event Subsystem

The Event system dramatically simplifies debugging of obscure or intermittent problems. Sixteen comparators and four trigger levels let you define complex, nested conditions to qualify breakpoints or trace. Forward and backward branching among trigger levels allows repetitive capture of isolated events in trace. SuperTAP's Event System provides you the ability to define up to eight active bus events at the same time to troubleshoot a complex condition. Two 32-bit event counters provide passcount information for triggers.

Furthermore, SuperTAP's NSE capability allows you to modify your triggers without stopping the target processor. Triggers include address match, address range, data match, data range, and bus cycle (read/write, halt, I/O, interrupt, DMA). Event actions include break emulation, change trigger level, count, assert trigger out, and Trace control.

Overlay Memory Subsystem

For convenient debugging of target PROM and RAM, you can map up to 1 MB of overlay memory to target addresses with an unlimited number of 2K blocks.

At full processor speed, overlay memory requires no wait states. Overlay is based on addresses and does not require chip selects. Attributes include target read/write, read-only or guarded, and overlay read/write or read-only. Guarded memory instantly detects corrupted pointers.

High-Speed Communications
In addition to high-speed RS-232 serial communications, SuperTAP supports high-speed RS-422 serial communications with actual transfer rates up to 7 MByte/min. For example, a 256K file downloads in just two seconds. These significantly shortened download times mean substantial productivity gains.

Hardware Diagnostics
Testing hardware integrity is simplified with stand-alone mode. In this mode, SuperTAP behaves just like a bare processor, eliminating the need to remove and replace chips for testing.

SuperTAP also lets you continue to communicate with and troubleshoot your target under conditions that cause other tools to crash. A second processor continuously monitors the emulation processor for RESET, HOLD, READY, Vcc, clock, and hung bus cycles. If anything goes wrong, SuperTAP not only will help you recover from the condition, but tell you why it happened.

Performance Analysis
With SuperTAP's powerful timestamp capability and interval timer, viewing system activity and code bottlenecks becomes easy.

For the most powerful software measurements, team SuperTAP with CodeTEST software verification tools. Combined, SuperTAP and CodeTEST become the ultimate embedded development platform, and are a must for industries requiring proof of compliance to specification such as in aerospace or medical fields. For commercial high volume product development, SuperTAP and CodeTEST can reduce the chance and expense of product recalls.

CodeTEST provides Performance Analysis—including function and task execution times as well as call-pair views—Coverage Analysis, Memory Allocation Analysis and Extended Trace Analysis—all non-sampled, all while the target runs in real time.

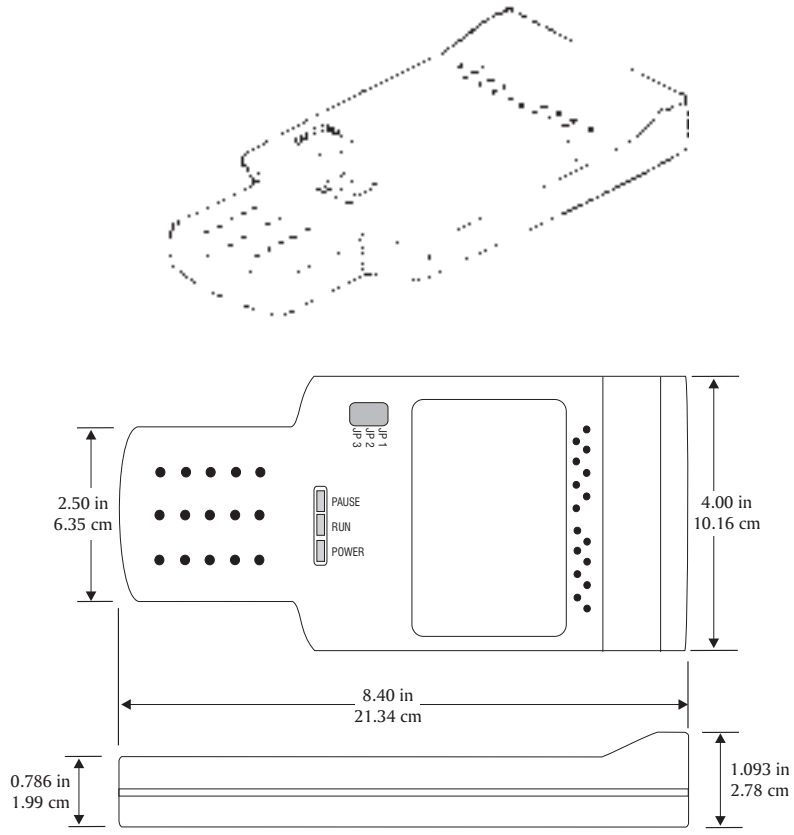
For more information about CodeTEST, refer to the CodeTEST data sheet.

Industry Leading Debugger
Applied has partnered with leaders in the industry to ensure your SuperTAP is part of a complete, integrated environment.

SuperTAP comes complete with debugger as well as cross-linker/locator tools to support the outputs of most leading X86 compilers.

For more information about SuperTAP, supported host operating systems, and user interface, see the SuperTAP debugger specification sheets.

CodeTEST Software Verification Tools bring a new dimension to software test and verification.



Dimensions of the SuperTAP Advanced Development Tool.

SPECIFICATIONS

Microprocessors Supported
AMD Am 186/188
AMD Am 186ED
AMD Am186/188EM, EMLV
AMD Am186/188ER
AMD Am186/188ES, ESLV

Speed
To 40MHz
3–5 volt operation at any speed
Selectable 8- and 16-bit bus

Packages Supported
PQFP clip-on
TQFP solder-down
PQFP solder-down

Communications
RS-232C host serial port (115K baud)
RS-422 serial interface (7 MByte/min)
(Both included in standard configuration)

SuperTAP Debugger
Paradigm DEBUG
MS-DOS / Windows 3.11 / *Windows 95/ *Windows NT / OS/2 compatible
*Call for availability

Software Tools Included
Paradigm LOCATE
Paradigm OMFCVT Conversion Utility

Macro Language
Full C-like expression language

Compilers Supported
Borland C/C++
Intel C-86
Intel PL/M-86
Microsoft C/C++
MetaWare High C/C++
MRI C86
Watcom C/C++
Other compilers that generate OMF symbolic format

Language Support
Assembler
C
C++
Pascal
PLM
Full C-like macro expression language

RTOS Support for System-Level Visualization
Paradigm RTOS Option:
AMX (Kadax)
SMX (Micro Digital)
RTXC (Embedded System Products, Inc.)
Nucleus (Accelerated Technology)
SuperTASK (U.S. Software)
RTKernel (OnTrack)
RTOS visibility at the SuperTAP level shows how the target, application, and RTOS interact with one another during execution in a thoroughly integrated, real-time environment; Displays real-time trace of RTOS activity, individual task context and other system structures (for more information, ask for the RTOS-Link data sheet)

Performance Analysis
Time interval trigger for statistical timing
Timestamp with scalable resolution

Overlay Memory
1 MB zero wait state to 40MHz
2K granularity
Attributes: target or overlay, read/write, read-only, guarded

Target Diagnostics
Monitor target Vcc, RESET, HOLD, and READY
Monitor target clock
Monitor bus timeout

Trace Subsystem
Featuring NSE™
64K deep x 80-bit wide real-time trace history including 20 address bits, 16 data bits, 4 execution bits, and timestamp
Display executed code in assembly and C-source with symbols or raw bus cycles
Trigger trace upon events
View dynamic trace display without stopping emulation
Timestamp from 25 ns to 8 hours

Event and Breakpoint Subsystem
Featuring NSE™ dynamic triggering
Unlimited software execution breakpoints
Hardware resources include:
- 8 hardware *execution* breakpoints
- 8 address access breakpoints
- 7 data access breakpoints
- Two 32-bit counters

Four trigger levels
Up to 8 inputs in one level
Up to 8 active bus events at one time

Triggering:
- Address match
- Address range
- Data match
- Data range
- Bus cycle (read, write, halt, I/O, interrupt, DMA)
- PINSTATE (INT 0–6, TIMERIN, TIMEROUT)
- External trigger

Event actions
- Break emulation
- Change trigger level
- Count
- Assert trigger out
- Trace one cycle/trace on/trace off

Minimum Host Requirements
486 44MHz PC or above
16550 UART
Win 3.11 or Win 95

Power Requirements
Powered from external supply
Input power 115 VAC, 47 Hz–63 Hz or 230 VAC, 47 Hz–63 Hz

Physical Specifications
Dimensions (LHW): 8.4 x 1.09 x 4.0" (21.43 x 2.78 x 10.16 cm)
Ambient humidity: 0–90% non-condensing
Operating temperature: 32–104° F (0–40° C)

U.S. and Canada
Applied Microsystems Corporation
5020 148th Avenue N.E.
Redmond, WA 98052
P.O. Box 97002
Redmond, WA 98073-9702
Tel: 425-882-2000
Toll-Free: 800-426-3925
Fax: 425-883-3049
Europe
Applied Microsystems Corporation Ltd.
AMC House, South Street
Wendover, Aylesbury
Buckinghamshire, HP22 6EF
United Kingdom
Tel: +44 (0)1296-625462
Fax: +44 (0)1296-623460
France
Applied Microsystems SARL
ZA1 de Courtaboeuf
7, Avenue des Andes
91952 Les Ulis Cedex
France
Tel: +33-1-64-463000
Fax: +33-1-64-460760
Germany
Applied Microsystems GmbH
Stahlgruberring 11a, 81829 Muenchen
Germany
Tel: +49 (0)89-427-4030
Fax: +49 (0)89-427-40333
Japan
Applied Microsystems Japan, Ltd.
Arco Tower 13 F
1-8-1 Shimomeguro, Meguro-ku
Tokyo 153
Japan
Tel: +81-3-3493-0770
Fax: +81-3-3493-7270

For more information: Call (800) 426-3925 (USA) or (425) 882-2000, e-mail info@amc.com, visit www.amc.com

Applied Microsystems
CORPORATION

CAD-UL Organon® XDB

For the SuperTAP™ Advanced Development Tool

A complete, integrated toolchain environment

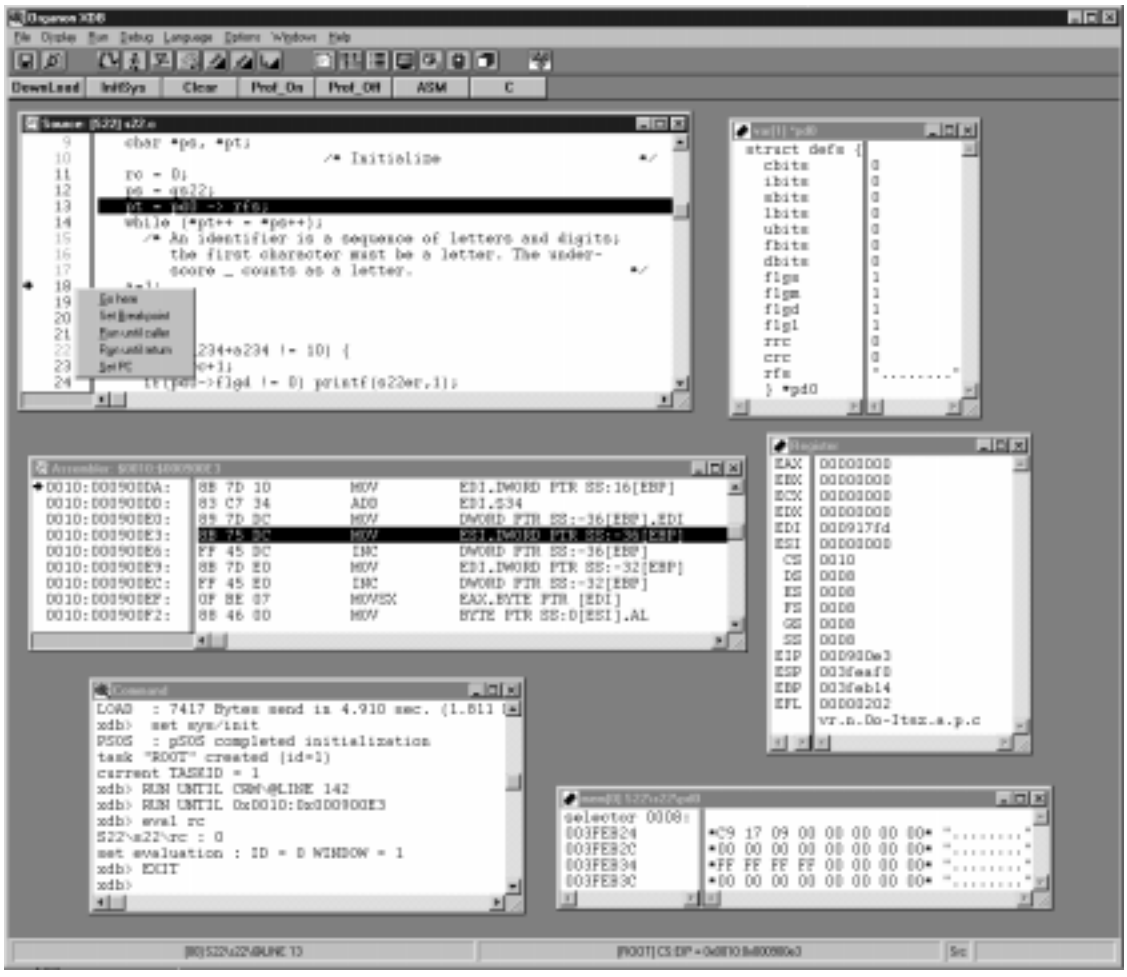
Organon XDB from CAD-UL offers full support of 16-bit and 32-bit Intel architectures on PC and Sun hosts. Support of CPU protection mechanisms are provided by supplying flat and segmented memory models and subsystems.

Support for 100+ built-in functions allows high level language access to all CPU functions; e.g., setglobaltable(), getlocaltable(), settaskregister(), causeinterrupt(), set_reg_eax().

Organon XDB debugger is packaged with LINK386 linker/locator system which supports allocation of descriptor tables, multitasking models, GATE definitions, absolute linkable and relocatable (loadable) code, and supports standard object formats.

Customized for SuperTAP

All of SuperTAP's features have graphical window displays and easy point-and-click access through the Organon interface including Trace, Event and Breakpoint system and Overlay. Organon XDB is available for 16-bit and 32-bit development and comes complete with locator that provides interoperability for a variety of compilers including CAD-UL, Borland, Intel, Microsoft, Watcom and other compilers that generate OMF symbolic format.



SPECIFICATIONS

Microprocessors Supported
AMD Am186/188EM, EMLV
AMD Am186/188ES, ESLV

Speed
To 40MHz
3–5 volt operation at any speed
Selectable 8- and 16-bit bus

Packages Supported
PQFP clip-on
TQFP solder-down
PQFP solder-down

Communications
RS-232C host serial port (115K baud)
RS-422 serial interface (7 MByte/min)
(Both included in standard configuration)
Optional Ethernet

SuperTAP Debugger and Hosts
CAD-UL Organon XDB
MS-DOS / Windows 3.1 / Windows 95/ Windows NT / OS/2 compatible
OSF-Motif, Sun-OS

Included with Debugger
CAD-UL Organon
LINK86 linker/locator

Complete Integrated Toolchain
Add CAD-UL Organon Compiler, Assembler, Linker and Libraries for a complete, integrated toolchain.

Macro Language
Full C-like expression language

Compilers Supported
Borland C/C++
CAD-UL CC86
Intel ASM-86
Intel PL/M-86
Intel iC-86
Watcom C/C++
Other compilers that generate OMF symbolic format

Language Support
Assembler
C
C++
Pascal
PLM

Performance Analysis
Timestamp with scalable resolution

Overlay Memory
1 MB zero wait state to 40 MHz
Unlimited number of 2K blocks
Attributes — target or overlay, read/write, read-only or guarded.

Trace Subsystem
Featuring NSE™
64K deep x 80 bit wide real-time trace history including address, data, status, and timestamp
Display executed code in assembly and C-source with symbols or raw bus cycles
Trigger trace upon events
View dynamic trace display without stopping emulation
Timestamp from 25 ns to 8 hours

Event and Breakpoint Subsystem
Featuring NSE™ dynamic triggering
Unlimited software execution breakpoints
Hardware resources include:
- 8 hardware *execution* breakpoints
- 8 address access breakpoints
- 8 data access breakpoints
- Two 32-bit counters

Four trigger levels
Up to 8 inputs in one level
Up to 8 active bus events at one time
Triggering:
- Address match
- Address range
- Data match
- Data range
- Bus cycle (read, write, halt, I/O, interrupt, DMA)
- PINSTATE (INT 0–6, TIMERIN, TIMEROUT)
- External trigger

Event actions
- Break emulation
- Change trigger level
- Count
- Assert trigger out
- Trace one cycle/trace on/trace off

Target Diagnostics
Monitor target Vcc, RESET, HOLD, and READY
Monitor target clock
Monitor bus timeout

Power Requirements
Powered from external supply
Input power 115 VAC, 47 Hz–63 Hz or 230 VAC, 47 Hz–63 Hz

Physical Specifications
Dimensions (LHW): 8.4 x .835 x 4.0" (21.43 x 2.12 x 10.16 cm)
Ambient humidity: 0–90% non-condensing
Operating temperature: 32–104° F (0–40° C)

ISO 9002 CERTIFIED

921-00000-00
00.00

U.S. and Canada
Applied Microsystems Corporation
5020 148th Avenue N.E.
Redmond, WA 98052
P.O. Box 97002
Redmond, WA 98073-9702
Tel: 425-882-2000
Toll-Free: 800-426-3925
Fax: 425-883-3049
Europe
Applied Microsystems Corporation Ltd.
AMC House, South Street
Wendover, Aylesbury
Buckinghamshire, HP22 6EF
United Kingdom
Tel: +44 (0)1296-625462
Fax: +44 (0)1296-623460
France
Applied Microsystems SARL
ZA1 de Courtaboeuf
7, Avenue des Andes
91952 Les Ulis Cedex
France
Tel: +33-1-64-463000
Fax: +33-1-64-460760
Germany
Applied Microsystems GmbH
Stahlgruberring 11a, 81829 Muenchen
Germany
Tel: +49 (0)89-427-4030
Fax: +49 (0)89-427-40333
Japan
Applied Microsystems Japan, Ltd.
Arco Tower 13 F
1-8-1 Shimomeguro, Meguro-ku
Tokyo 153
Japan
Tel: +81-3-3493-0770
Fax: +81-3-3493-7270

For more information: Call (800) 426-3925 (USA) or (425) 882-2000, e-mail info@amc.com, visit www.amc.com