AMD-K6®

Processor Revision Guide

Model 7

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AMD-K6® Processor Revision Guide - Model 7

The purpose of the *AMD-K6® Processor Revision Guide - Model 7* is to communicate updated product information on the AMD-K6 processor to designers of computer systems and software developers. Model 7 of the AMD-K6 processor is manufactured in 0.25-micron process technology. This guide consists of four major sections:

- **Product Marking Identification:** This section provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification.
- **Specification Changes/Clarifications:** This section provides changes, additions, and clarifications to product specifications.
- **Technical and Documentation Support:** This section provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

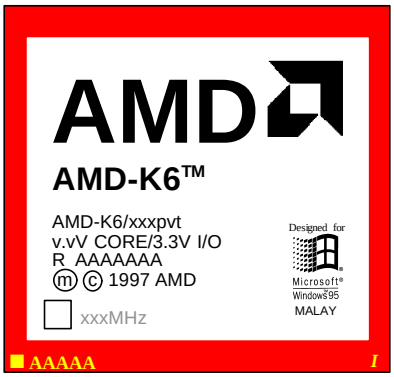
Revision Guide Policy

At times, AMD identifies deviations or changes to the specification of the AMD-K6 processor. These are documented in the *AMD-K6 Processor Revision Guide* as errata or specification changes/clarifications and are available to anyone who requests the information. The descriptions are written to assist system and software designers in using the AMD-K6 processor. In addition, any corrections to AMD's published documentation on the AMD-K6 processor are included. The errata and specification changes are the result of extensive testing and validation that is done for all AMD products. AMD works closely with system and software designers to ensure the appropriate workarounds or changes are implemented to avoid impact to PC users.

The *AMD-K6 Processor Revision Guide* is made publicly available to all who are interested during the third week of each month. All issues that have been resolved and communicated to AMD's customers are included in this release.

1 Product Marking Identification

1.1 Production Marking



Ceramic Pin Grid Array (CPGA)

(Packages Not Drawn to Scale)

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xxxpvt = OPN, where:

- xxx = Operating Frequency
- p = Package Type
  - A = 321-pin PGA
- v = Operating Voltage
  - F = 2.1-2.3V Core/3.135-3.6V I/O
- t = Maximum Case Temperature
  - R = 70°C

v.vV = Core Voltage, where:

- 2.2V = 2.2V Component

R AAAAAAA = Revision, where:

- R = Revision
  - A = Revision A
  - B = Revision B
  - etc.
- AAAAAAA = Internally-Defined

2 Product Errata

This section documents AMD-K6 processor product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2-1 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping. Shading within the table indicates an addition or modification from the previous release of this document.

Table 2-1. Cross-Reference of Product Revision to Errata

Erratum Number	Description	Rev A
	Test and Debug	
2.1.1	Built-In Self-Test (BIST)	X
2.1.2	Boundary-Scan Test Access Port (TAP)	X
	System Bus	
2.2.1	Drive Strength Selection	X
2.2.2	HLDA Assertion Delayed by One Clock	X
2.2.3	Output Min Valid Delay Timings for 66-MHz & 60-MHz Bus Operation	X
2.2.4	Input & Output Leakage Current	X
	Interrupts and Exceptions	
2.3.1	Memory Accesses Using Null Selectors	X
2.3.2	Exception Priority of MMX Instructions	X
	Reset and Initialization	
2.4.1	Initial Power-On Reset - TDI Requirement	X
	Shading indicates additions or modifications from the previous release of this document	

2.1 Test and Debug

2.1.1 Built-In Self-Test (BIST)

Products Affected. A stepping

Normal Specified Operation. Following the falling transition of RESET, the processor unconditionally runs its BIST.

Non-conformance. BIST is not supported.

Potential Effect on System. The L1 caches are not tested after RESET.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.1.2 Boundary-Scan Test Access Port (TAP)

Products Affected. A stepping

Normal Specified Operation. The processor supports the boundary-scan Test Access Port (TAP) as defined by the *IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990)* specification.

Non-conformance. The boundary-scan TAP is not supported.

Potential Effect on System. Boundary scan testing cannot be performed. This erratum does not affect the functional operation of a system.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.2 System Bus

2.2.1 Drive Strength Selection

Products Affected. A stepping

Normal Specified Operation. The processor samples the $\overline{\text{BRDYC}}$ input during the falling transition of RESET to configure the drive strength of A20–A3, $\overline{\text{ADS}}$, $\overline{\text{HITM}}$, and W/$\overline{\text{R}}$. If $\overline{\text{BRDYC}}$ is sampled asserted during the fall of RESET, these particular outputs are configured using a higher drive strength than the standard drive strength. If $\overline{\text{BRDYC}}$ is sampled negated during the fall of RESET, the standard drive strength is selected for these particular outputs.

Non-conformance. If $\overline{\text{BRDYC}}$ is sampled asserted during the fall of RESET, all output drivers are configured using the higher drive strength.

Potential Effect on System. Using the higher strength drive configuration can affect signal quality by resulting in additional overshoot or undershoot.

Suggested Workaround. Use the standard drive configuration. With few exceptions, most board designs require the standard drive configuration.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.2.2 HLDA Assertion Delayed by One Clock

Products Affected. A stepping

Normal Specified Operation. If $\overline{\text{BOFF}}$ and HOLD are sampled asserted on the same clock edge that negates $\overline{\text{ADS}}$, the processor asserts HLDA one clock edge after HOLD is sampled asserted.

Non-conformance. If $\overline{\text{BOFF}}$ and HOLD are sampled asserted on the same clock edge that negates $\overline{\text{ADS}}$, the processor asserts HLDA two clock edges after HOLD is sampled asserted.

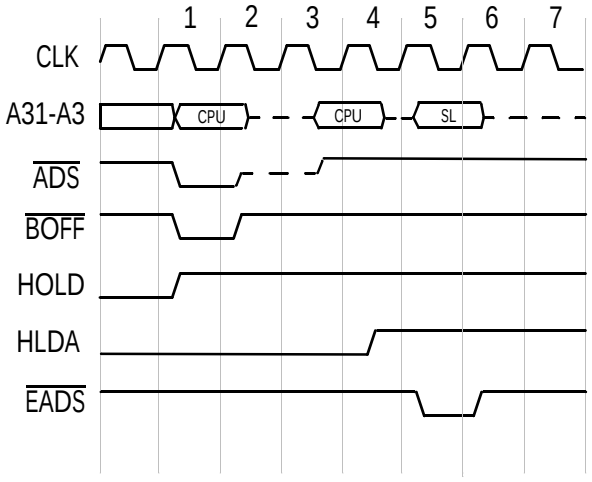
Potential Effect on System. There are three potential effects of this erratum to consider:

- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of one clock, anticipates the assertion of HLDA in clock 3 (see Figure 1)—which is the normal specified operation—and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 3, then the processor will not sample $\overline{\text{EADS}}$ asserted. In addition, address bus contention will occur in clock 3.
- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of two clocks, anticipates the assertion of HLDA in clock 3, and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 3, then the processor will not sample $\overline{\text{EADS}}$ asserted. (No address bus contention occurs in this case.)
- If the system logic asserts $\overline{\text{BOFF}}$ for a duration of one clock, anticipates the assertion of HLDA in clock 3, and drives the address bus and $\overline{\text{EADS}}$ for an inquire cycle in clock 4, then address bus contention may occur in clock 4. (The processor will sample $\overline{\text{EADS}}$ asserted in this case.)

If the processor does not sample $\overline{\text{EADS}}$ asserted during an inquire cycle, cache/memory incoherency will occur. Address bus contention can affect the reliability of the processor and the system logic.

Suggested Workaround. The system logic must sample the assertion of HLDA before asserting $\overline{\text{EADS}}$ and driving the address bus for an inquire cycle—as shown in clock 5 of Figure 1.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.



CPU: Processor is driving A31–A3
SL: System Logic is driving A31–A3

Figure 1. AMD-K6 Processor Assertion of HLDA Due to Simultaneous $\overline{\text{BOFF}}$/HOLD Assertion

2.2.3 Output Min Valid Delay Timings for 66-MHz & 60-MHz Bus Operation

Products Affected. A stepping

Normal Specified Operation. The minimum valid delay for all output signals is specified between 1.0 ns to 1.3 ns.

Non-conformance. The minimum valid delay for all output signals is 700 ps.

Potential Effect on System. Minimum valid delay timings directly affect hold times to the system logic. If these hold time requirements are violated, the functional operation of the system in unpredictable. This specification erratum should be fully validated on targeted system designs to ensure that all timing requirements are satisfied.

This erratum has not been observed to adversely affect system functionality.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.2.4 Input & Output Leakage Current

Products Affected. A stepping

Normal Specified Operation. The maximum input (I_{LI}) and output leakage (I_{LO}) current is specified as +/-15µA.

Non-conformance. The maximum input (I_{LI}) and output leakage (I_{LO}) current is +200µA/-250µA.

Potential Effect on System. The outline below lists the potential effects on a system due to excessive negative and positive leakage. This specification erratum should be fully validated on targeted system designs to ensure functional operation.

Excessive negative leakage current may...

- for I/O pins with weak pull-downs, cause intended Low signals to be detected above Input Low Voltage thresholds (V_{IL} = 0.8V).
- slightly increase the signal fall-time and slightly decrease the signal rise-time.
- increase in-circuit test delays for a High driven, pull-down pin to reach a safe Low voltage level when Tri-stated.
- slightly increase the power consumption for I/O pins with external pull-down resistors (greater impact in low-power states).

Excessive positive leakage current may...

- for I/O pins with weak pull-ups, cause intended High signals to be detected below Input High Voltage thresholds (V_{IH} = 2.0V).
- slightly increase the signal rise-time and slightly decrease the signal fall-time.
- increase in-circuit test delays for a Low driven, pull-up pin to reach a safe High voltage level when Tri-stated.
- slightly increase the power consumption for I/O pins with external pull-up resistors (greater impact in low-power states).

Identifying processor Input pins, critical by design, with weak pull-up or pull-down resistors and limiting the amount of leakage current allowed on these pins ensures signal voltage levels do not drift above V_{IL} or below V_{IH} levels due to leakage current. Subsequent to the +200µA/-250µA production test on I/O pins, AMD has implemented a tighter test to screen Input pins potentially affected by this erratum. Validating, through system tests, that signal timings remain within system logic and processor requirements ensures signal timings are not adversely affected by leakage current.

This erratum has not been observed to adversely affect system functionality.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.3 Interrupts and Exceptions

2.3.1 Memory Accesses Using Null Selectors

Products Affected. A stepping

Normal Specified Operation. An attempt to access memory with a segment register that contains a null selector causes a general protection fault to occur.

Non-conformance. On entering System Management Mode (SMM), the processor saves its state into the SMM state-save area. The processor returns from SMM when it executes the RSM (resume) instruction from within the SMM service routine. If any of the segment registers contains a null selector on entering SMM, then after executing the RSM instruction, the internal state bit associated with the corresponding segment descriptor is erroneously set to indicate that this segment is readable. In this case, the processor does not generate a general protection fault when attempting to read memory using a null selector, but instead allows the memory read cycle to occur without generating an exception.

Potential Effect on System. Unless an application is errant, an application generally does not access segments using null selectors. However, an application that depends on the processor to generate a general protection fault if a null selector is used will not execute successfully.

This erratum has not been observed to adversely affect a system. It was detected by design inspection.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

2.3.2 Exception Priority of MMX Instructions

Products Affected. A stepping

Normal Specified Operation. The processor supports the generation of invalid opcode exceptions for the MMX instruction set.

Non-conformance. If the TS bit of Control Register 0 (CR0) equals 1, the processor generates a "device not available" (DNA) exception instead of an invalid opcode exception when attempting to execute an MMX instruction that uses the following invalid opcodes:

- Opcode equals 0F_71h and Mod R/M[5:3] not equal to (010b, 100b, or 110b)
- Opcode equals 0F_72h and Mod R/M[5:3] not equal to (010b, 100b, or 110b)
- Opcode equals 0F_73h and Mod R/M[5:3] not equal to (010b or 110b)
- Opcode equals (0F_71h, 0F_72h, or 0F_73h) and Mod R/M[7:6] not equal to 11b

Note: These opcodes are invalid Mod R/M combinations of the packed immediate shift MMX instructions.

Potential Effect on System. Unless the software is errant, an invalid opcode exception will not occur. However, if an application unintentionally uses one of the above specific invalid opcodes, the processor generates a DNA exception. If the DNA exception handler sets the TS bit of CR0 to 0 and returns to the invalid opcode, the processor generates an invalid opcode exception.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor

2.4 Reset and Initialization

2.4.1 Initial Power-On Reset - TDI Requirement

Products Affected. A stepping

Normal Specified Operation. During the initial (cold) power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK, Vcc2, and Vcc3 reach specification before it is negated.

Non-conformance. To ensure that the processor is properly reset during power-on reset, the Test Data Input (TDI) signal must be High.

Potential Effect on System. If TDI is Low during power-on reset, the processor is not reliably reset. If reset does not successfully complete, the processor hangs.

Suggested Workaround. Ensure that TDI is High during power-on reset. If TDI is left unconnected on the board, the processor's internal pull-up on TDI ensures that TDI is High during reset.

Resolution Status. This erratum will be corrected in a future stepping of the AMD-K6 processor.

3 Specification Changes/Clarifications

This section documents AMD-K6 processor specification changes and clarifications. The changes/clarifications are divided into categories to assist referencing particular changes. A unique tracking number for each change/clarification has been assigned within this document for user convenience in tracking the specification change/clarification within specific revision levels. Table 3-2 cross-references the revisions of the processor to each specification change/clarification. An "X" indicates that the specification change/clarification applies to the stepping. The absence of an "X" indicates the specification change/clarification does not apply to the stepping.

Table 3-2. Cross-Reference of Product Revision to Specification Change/Clarification

Change Number	Description	Rev A
	Interrupts and Exceptions	
3.1.1	Recognition of External Hardware Interrupts During I/O Read Cycle	X
	Instructions	
3.2.1	SYSCALL and SYSRET	X
	Shading indicates additions or modifications from the previous release of this document	

3.1 Interrupts and Exceptions

3.1.1 Recognition of External Hardware Interrupts During I/O Read Cycle

New Specification Applies to: A and subsequent steppings

Previous Operation. For I/O Reads, the AMD-K6 processor waits for preceding instructions to complete before executing the I/O Read instruction. However, there is no serialization for succeeding instructions. This means that succeeding instructions can be executed in parallel with the I/O Read. As a result, external interrupts may not be recognized and serviced before succeeding instructions are completed.

New Operation. For I/O Reads, the AMD-K6 processor waits for preceding instructions to complete before executing the I/O Read instruction and it serializes succeeding instructions. This means that the I/O Read instruction completes before any succeeding instructions are executed. Such serialization allows for external interrupts, asserted during the I/O cycle, to be recognized and serviced before any dependent instructions are executed.

Implication. The previous and new operation has no implication for software and hardware that are designed to the Socket 7 specification, which states that IN instructions are not fully serialized.

3.2 Instructions

3.2.1 SYSCALL and SYSRET

New Specification Applies to: A and subsequent steppings

Previous Operation. The AMD-K6 processor supports the SYSCALL and SYSRET Extensions, which provide a fast method for entering and exiting an operating system. Bit 10 of the Extended Feature Flags (Function 8000_0001h of the CPUID instruction) is set to 1 to indicate support for the SYSCALL and SYSRET Extensions. Bit 11 of the Extended Feature Flags is Reserved.

New Operation. Bit 11 of the Extended Feature Flags indicates whether support for the SYSCALL and SYSRET Extensions exists—if bit 11 is set to 1, then the SYSCALL and SYSRET Extensions are supported; if bit 11 is set to 0, then the SYSCALL and SYSRET Extensions are not supported.

Implication. Since no operating systems currently utilize these instructions, there is no implication to existing software. For the future, the Extended Feature flags must be read and interpreted as defined in *New Operation* in order to determine if a specific stepping of the AMD-K6 processor supports the SYSCALL and SYSRET Extensions.

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-K6 processor:

- AMD-K6® Processor Data Sheet (order# 20695)
- AMD-K6® Processor Multimedia Technology (order# 20726)
- AMD K86™ Family BIOS and Software Tools Developers Guide (order# 21062)
- AMD K86™ Family BIOS Design Application Note (order# 21329)
- AMD Processor Recognition Application Note (order# 20734)
- Implementation of Write Allocate in the K86 Processors (order# 21326)
- AMD-K6® Processor Thermal Solution Design Application Note (order# 21085)
- AMD-K6® Processor Power Supply Design Application Note (order# 21103)
- AMD-K6® Processor I/O Model Application Note (order# 21084)
- AMD-K6® Processor V_{CC2} Voltage Detection Application Note (order# 21635)

For the latest updates, refer to www.amd.com and download the appropriate files.