Automatic Voltage Detection/Regulation by Planars or Motherboards

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Application Note

Introduction

This paper explains the method used by planar designers to automatically detect the Vcc voltage needed by the microprocessor which is placed into the upgradable ZIF (Zero-Insertion Force) sockets that are located on many of today's planars or motherboards.

Computer designers today are very conscious of power consumption; therefore, every effort is made to achieve maximum performance with minimal power usage. One way to achieve minimal power consumption is to lower the voltage level that is needed by the microprocessor in a computer system. Instead of using the once standard 5-volt supply voltage, many processors today use a 3.3-volt or 3.6-volt input to their power pins.

This difference in voltages, however, can pose a serious problem to end-users who wish to upgrade their system. For instance, if someone is currently using a 5-volt Intel 486SX microprocessor in their system, and they want to upgrade to a 3.3-volt Intel®486DX4 processor, there is a potential that the customer may not realize that a voltage difference exists between the two parts. By simply plugging the lower voltage part into the higher voltage socket, the end-user could destroy their new 486DX4 part because the technology in the new part cannot handle 5 volts on its power pins.

To eliminate this potential for error, Intel added a VOLTDET to the 486DX4 processors. This pin is referenced as pin S4 on the 168-pin PGA package. Pin S4 is an output of the microprocessor which signals the planar that either a 3-volt supply or a 5-volt supply is needed for the processor's Vcc pins. If this signal is a logic '1', then a 5-volt supply is selected; if it is a logic '0', then a 3-volt supply is selected by the planar logic. By default, many planars automatically supply 5 volts to the ZIF (Zero-Insertion Force) socket unless a 3-volt part (which has a VOLTDET pin) is placed into the socket.

The 3-volt Ibm 486DX2 processors do not have a VOLTDET pin. There must be jumpers on the planar which can be used to "manually" select the voltage supplied to the upgraded

processor's Vcc pins. Even though these microprocessors do not have a VOLTDET pin, many planar designers may wish to accommodate both a IBM 486DX2 processor and an Intel 486DX4 processor in their planar designs. The S4 pin, however, is reserved as the INVAL pin for the write-back cache on Ibm. Thus, application concerns arise.

There are two possible solutions to this dilemma: the first method allows for a relatively easy design which will only make the 3-volt Ibm S4 pin compatible with the Intel part; the other also allows the planar designers the use of the write-back cache feature on the Ibm processor.

Design For Intel Compatibility Only

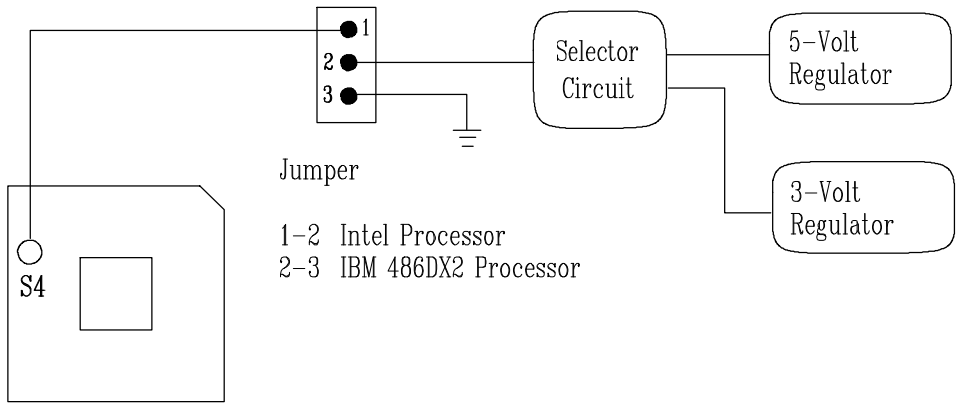
For a quick, easy design which allows a 3-volt Ibm processor to be plug-compatible (with respect to the S4 pin only) to the Intel 486DX4 processor, the planar's S4 pin via can be connected to ground.

Since the planar logic will select a 3-volt regulator if the S4 line is logic '0', connecting this signal line to ground will allow the correct voltage to be supplied to the Ibm processor. Care must be taken, however, to insure that the processor's S4 pin is not electrically connected to the S4 via because of the IBM 486DX2 internal pull-up resistor on the INVAL pin.

This suggested design, however, eliminates the designer's ability to utilize the write-back cache feature on the IBM processor. To insure that the write-back features are not initialized, the following must be true:

1. CR0 Register, bit 29 (NW) must be set to a logic '0'
2. CCR2 Register, bit 1 (WBAK) must be set to a logic '0'

A suggested circuit for this design is as follows:



Design for Intel Compatibility and Use of Write-Back Cache

To achieve optimal performance on the Ibm processor, the designers may still wish to utilize the processor's write-back cache feature.

This design is a little more involved than the previous design because the planar designer must insure that the write-back cache pins are properly connected to the planar's chipset. The chipset must also support a write-back cache.

Jumpers will still be used. Connecting the S4 pin via to ground is still necessary for the planar's voltage detection circuit. Another jumper, however will be necessary to allow a direct path to the detection circuit for the Intel part's VOLTDET pin to function properly.

The I/O pins which are associated with write-back are:

1) HITM# - Hit on Modified Data
2) INVAL - Invalidate RequestA suggested circuit for this design is as follows