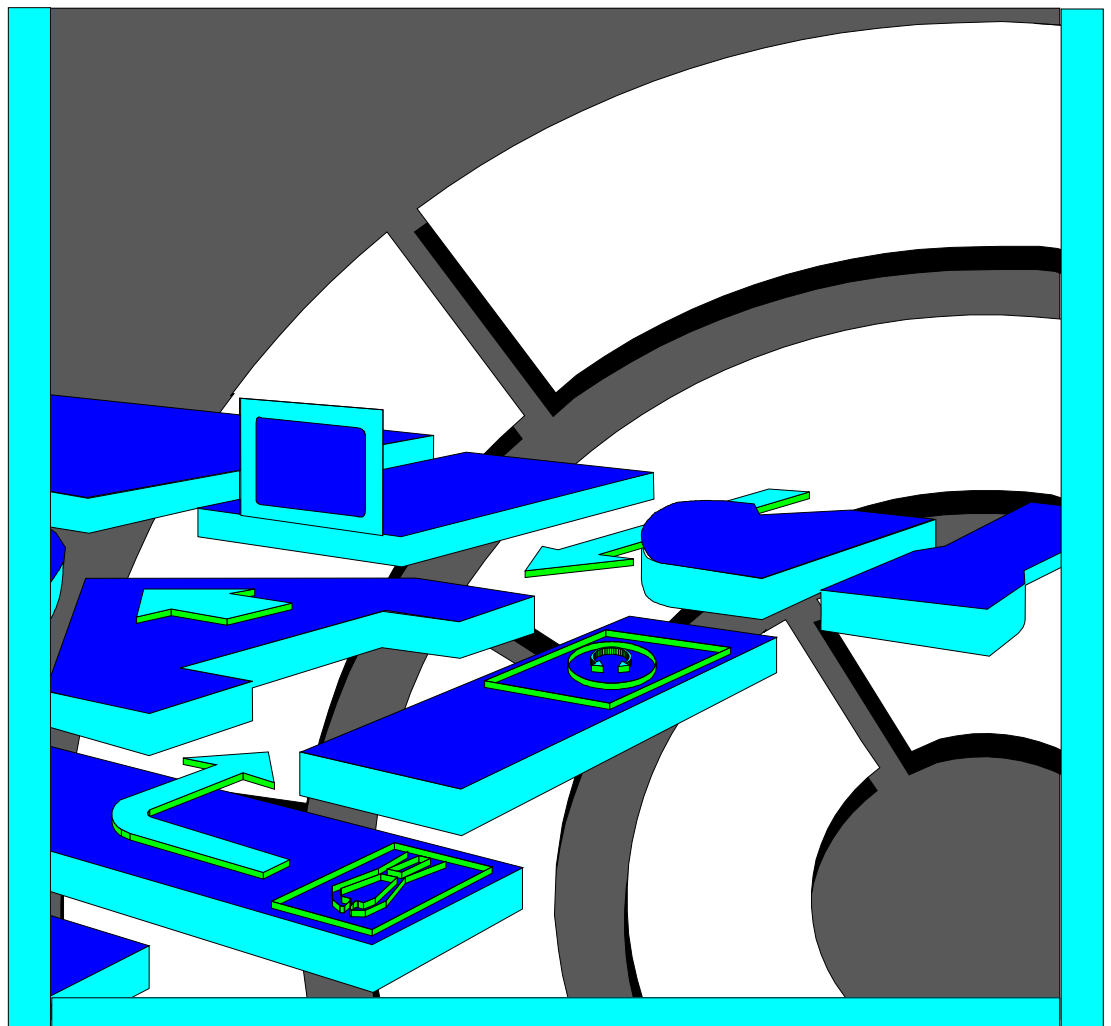IBM ARTIC960 and IBM ARTIC960 PCI
Co-Processor Platforms

DAP2-0000-01

Application Interface Board
Developer's Guide

IBM

IBM ARTIC960 and IBM ARTIC960 PCI
Co-Processor Platforms

Application Interface Board
Developer's Guide

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┌─ Important ──────────────────────────────────────────────────────────────────┐
│                                                                              │
│  Before using this information and the product it supports, read the information under "Notices" on page xi. │
│                                                                              │
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Third Edition (July 1996)

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Notices

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About This Book

This publication is intended for use by developers of application interface boards (AIBs) that attach to IBM ARTIC960 and ARTIC960 PCI Co-Processor Platforms. It contains specifications and other technical information that must be adhered to when developing new AIBs. This information provides the hardware and the software developer with AIB design requirements and a collection of productivity tools to aid in developing an AIB.

Note: Unless noted otherwise, *ARTIC960 Co-Processor Platform* is used to denote both the ARTIC960 and ARTIC960 PCI co-processor adapters.

The objectives of this publication are to:

- Describe the necessary components of the AIB.

- Describe the "Common Front End" (CFE) that must be designed into the AIB, including the function of its required components.

- Describe the ROM Bus that must be designed into the AIB.

- Explain the ROM interface and the AIB ROM requirements.

- Describe the interaction of the AIB and the IBM ARTIC960 Co-Processor Platform.

- Provide other descriptions and data related to the AIB configuration, component layout, circuitry, functions, hardware interfaces, and programming considerations.

Audience

The information in this publication is both introductory and for reference use. It is intended for hardware and software designers, programmers, engineers, and anyone with a knowledge of electronics and/or programming who wishes to understand the use and the operation of the AIB.

It is assumed the reader is familiar with the IBM ARTIC960 Co-Processor Platform, as well as the computer system in which it is installed, the applications in use, and programming. Therefore, terminology is not explained in this book, except for terms that may have different meanings.

Note: Detailed programming information for the co-processor platform can be found in the *IBM ARTIC960 Co-Processor Platforms Programmer's Guide and Reference*.

Organization

The information contained in this publication is organized as follows:

- *Chapter 1. IBM ARTIC960 Co-Processor Platform Components* provides an overview of the IBM ARTIC960 Co-Processor Platform and its subsystems. The subsystems include the Microprocessor, Read Only Memory (ROM), Memory Controller, System Bus Interface.

- *Chapter 2. Co-Processor Platform Interrupt Controller Subsystem* contains an overview of the IBM ARTIC960 Co-Processor Platform interrupt structure and the interrupt controller chip.

- *Chapter 3. AIB Architecture* describes the IBM ARTIC960 Co-Processor Platform address mapping and how the AIB maps into the base architecture.

- *Chapter 4. AIB Interface* describes the AIB interface signal set, including the connector pinout.

- *Chapter 5. ROM Bus Timings* describes the timing for reading and writing the ROM bus.

- *Chapter 6. Common Front End (CFE)* covers the CFE bus timings and the CFE design recommendations.

- *Chapter 7. AIB Hardware Design Application Notes* contains design hints and recommendations for the hardware designer.

- *Chapter 8. AIB ROM* provides a detailed discussion of the AIB ROM requirements, the AIB/Base ROM interface, the ROM table, and the error reporting mechanisms.

- *Chapter 9. AIB Diagnostics* describes how to obtain assistance developing AIB diagnostic routines.

- *Chapter 10. AIB Physical Characteristics* identifies the component height restrictions of the AIB, and illustrates the hole pattern and dimensions of the AIB connector.

- *Appendix A. Design Workbook for Generic CFE Devices* presents generic full-function CFE control state machines.

Conventions and Symbols

The Conventions and symbols used in this publication are as follows:

- All counts in this document are assumed to start at zero.

- All bit numbering conforms to the industry standard of the most significant bit having the highest bit number. Bytes are numbered in descending order from right to left, which results in the most significant byte of a word having the highest address.

```
                                                    0
                                           ┌──────────────────┐
                                           │7                0│
                                           └─┴─┴─┴─┴─┴─┴─┴─┴──┘

                                  1                  0
                         ┌──────────────────┬──────────────────┐
                         │      MSB         │       LSB        │
                         │15               8│7                0│
                         └─┴─┴─┴─┴─┴─┴─┴─┴──┴─┴─┴─┴─┴─┴─┴─┴─┴──┘

           3                  2                  1                  0
  ┌──────────────────┬──────────────────┬──────────────────┬──────────────────┐
  │      MSB         │                  │                  │       LSB        │
  │31             24│23              16│15               8│7                0│
  └─┴─┴─┴─┴─┴─┴─┴─┴──┴─┴─┴─┴─┴─┴─┴─┴─┴──┴─┴─┴─┴─┴─┴─┴─┴─┴──┴─┴─┴─┴─┴─┴─┴─┴─┴──┘
```
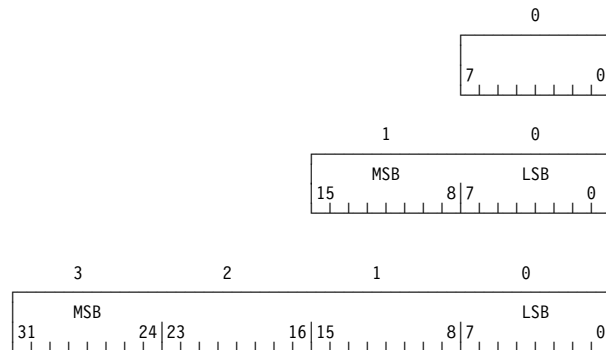
- All numeric parameters and command line options are assumed to be decimal values unless otherwise noted.

- To pass a hexadecimal value for any numeric parameter, the parameter should be prefixed by **0x** or **0X**. The numeric parameters **16**, **0x10**, and **0X10** are all equivalent.

- All representations of bytes, words and double words are in the Intel(C) format.

Timing Diagram Notations

The following abbreviations/symbols are used in the timing sections of this manual:

↑   Rising edge of PCLK

                    Steady state either high or low

                    Transition state

                    Tri-state going to transition state

IBM ARTIC960 Co-Processor Platform Developer's Kit — Content

The Developer's Kit is a set of publications and programs designed to help ARTIC960 AIB software developers develop for the ARTIC960 platform. The following items make up the Developer's Kit:

- *IBM ARTIC960 Co-Processor Platform Hardware Technical Reference* presents technical details of the adapter's system, options, and hardware interfaces. It provides descriptions and data related to the card configuration, functions, hardware interfaces, and programming considerations.

- *IBM ARTIC960 Co-Processor Platforms Programmer's Guide and Reference* provides an overview of both the adapter kernel support and the operating system support. It also describes the associated processes and utilities, as well as each of the services provided by the system unit support and the adapter kernel support.

- *IBM ARTIC960 Co-Processor Platform Application Interface Board Developer's Guide* provides the hardware and the software developer with AIB design requirements, and a collection of productivity tools to aid in the development of an AIB.

- A set of operating system packages, each containing sample programs and utilities to support the development of system unit and adapter applications. These packages are to be used with the *IBM ARTIC960 Co-Processor Platforms Programmer's Guide* and the *IBM ARTIC960 Co-Processor Platform Application Interface Board Developer's Guide*.

You can obtain these publications in PostScript format from the World Wide Web (WWW) at:

```
http://wwprodsoln.bocaraton.ibm.com/artic/
```

If you do not have access to the WWW, or you cannot print PostScript files, you can obtain these publications from the no-fee Developer's Assistant Program (DAP), which also provides technical question-and-answer (Q&A) services supported by telephone and E-mail, as explained under "Developer's Assistance Program."

Developer's Assistance Program

- In addition to the *Developer's Kit*, further programming and hardware development assistance is provided by the IBM ARTIC960 Developer's Assistance Program (DAP). The DAP will provide, via phone and electronic communications, on-going technical support—such as sample programs, debug assistance, and access to the latest microcode upgrades.

  For more information or to activate your **free** IBM ARTIC960 DAP membership, **call 1-800-IBM-3333** and ask for **ARTIC 160**. In Canada, call 1-800-465-1234. On E-mail, specify **artic@vnet.ibm.com**.

Reference Publications

You may need to use one or more of the following publications for reference:

- Operating and Installation documentation provided with your computer system.

- IBM Operating System/2 documentation.

- IBM Advanced Interactive Executive documentation.

- *IBM ARTIC960 Co-Processor Platform Guide to Operations*
  IBM ARTIC960 PCI Co-Processor Platform Guide to Operations.
  These manuals contain a description of the appropriate co-processor platform,
  instructions for physically installing the adapter, procedures for installing and
  setting up the operating system, configuration information, parts listings, and a
  Symptom-to-FRU Index Supplement.

- *IBM Application Interface Board Supplement(s)* to the Guide to Operations for
  the IBM ARTIC960 Co-Processor Platform and ARTIC960 PCI Co-Processor
  Platform.
  Each Supplement contains a description of an IBM-developed AIB, instructions
  for installing the AIB, interface connector information, and interface cable
  details.

- *IBM Application Interface Board Hardware Maintenance Libraries*.
  Each AIB Library contains one or more wrap plugs that are used during
  diagnostic testing to wrap selected interface lines of an IBM-developed AIB and
  the associated Interface Cable. Also included are removal and replacement
  procedures for field-replaceable units (FRUs), parts listings, and a
  Symptom-to-FRU Index Supplement. Most AIB Libraries include a diagnostic
  diskette that is used to isolate a symptom to a failing FRU.

Chapter 1. IBM ARTIC960 Co-Processor Platform Components

This chapter briefly describes the co-processor platform hardware. It begins with a high-level overview and then explains the functions of the individual components.

The following terms are used throughout this manual:

AIB　　Application Interface Board. This board attaches to the co-processor platform through the AIB Connector. This board also can be referred to as the daughter card.

AIB Interrupts

These are the interrupts from the AIB that go to the co-processor platform's interrupt controller.

Base Card

This is the IBM ARTIC960 Co-Processor Platform.

CFE Local Bus

This is the bus connecting the ARTIC 32-bit Memory Controller Chip, the System Bus Interface Chip, and the AIB connector. This bus supports the Common Front End 32-bit signal set.

PCI　　Peripheral component interconnect.

System Bus Interface Chip (SBIC)

There are two versions of the System Bus Interface Chip. One supports Micro Channel applications; the other supports PCI bus applications. Where possible, *System Bus Interface Chip* is used, and specific differences between Micro Channel and PCI applications are noted.

Functional Block Diagram
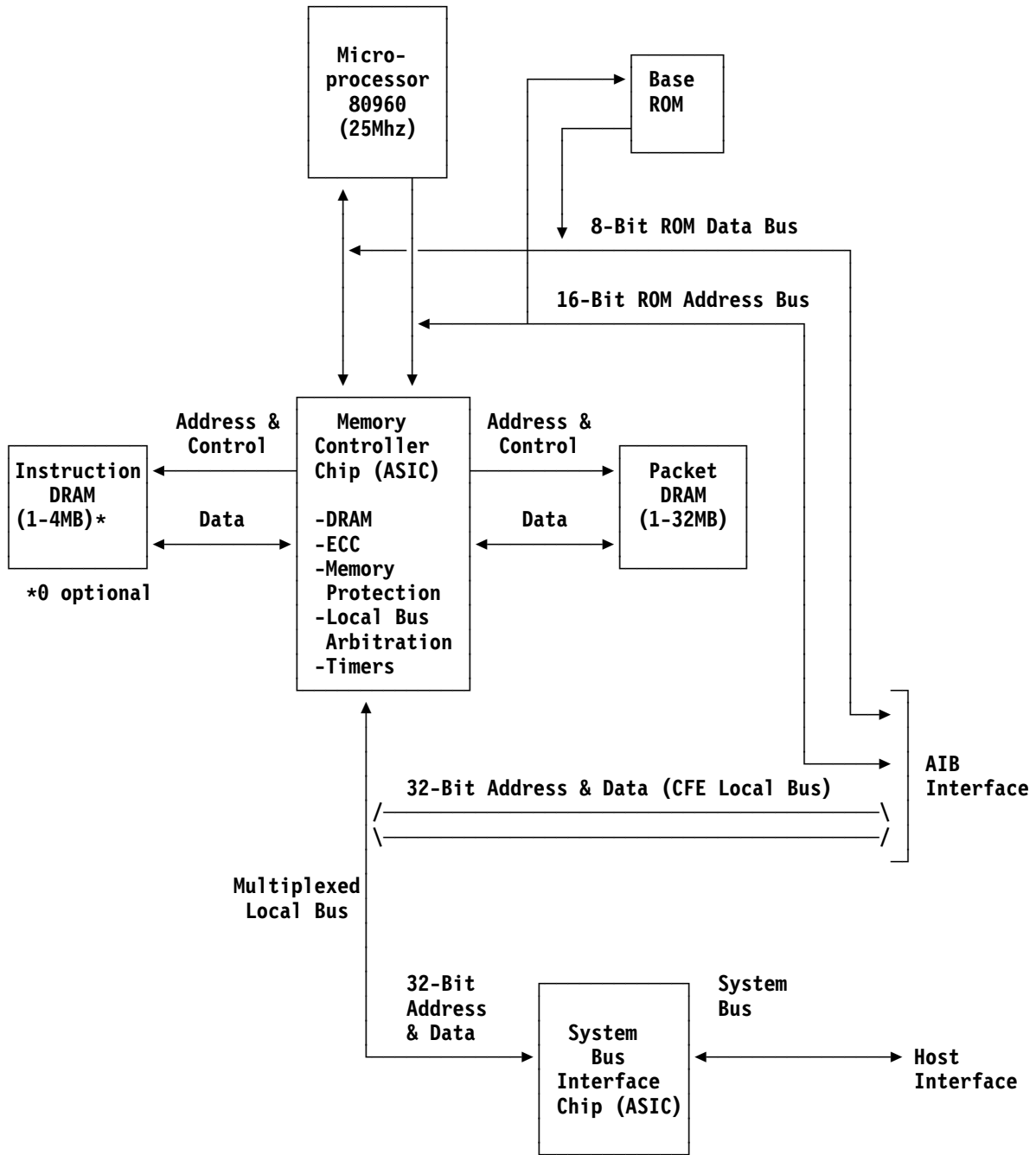
Figure   1-1. IBM ARTIC960 Co-Processor Platform Block Diagram

Microprocessor

The Intel 80960C-Series processor is used on the co-processor platform. Earlier co-processor platforms use the CA version and later platforms use the CF version.

The Intel 80960C-Series processor provides the following:

- Operation at 25MHz
- CMOS technology
- Approximately 7 to 10 MIPS, based on instruction mix
- 1KB/4KB, on-chip, two-way set associative instruction cache
- 1KB, on-chip, high-speed SRAM
- Vectored interrupt support
- High bandwidth, 16-byte bursting bus

The 80960 has access to memory, the local CFE bus, and the ROM bus. The AIB can be accessed by the 80960, through the CFE bus or the ROM bus.

Memory

Both DRAM and ROM memory are supported on the co-processor platform. Since the entire address space of the 80960 is memory mapped, all registers appear as memory.

Dynamic Random Access Memory (DRAM)

The co-processor platform can be configured with either one or two DRAM banks. The execution/packet memory is the default memory bank. The granularity of this memory is 1, 2, 4, 8, 16, or 32 megabytes (MB). The co-processor platform also supports an optional execution-only (instruction memory) DRAM bank for those applications requiring higher I/O throughput and/or processing bandwidth. This memory can have granularities of 1 or 4MB. The starting address for packet memory is 512MB (2000 0000h), and the starting address for instruction memory is 544MB (2200 0000h). This information is stored in the memory configuration register. All DRAM memory on the adapter is Error Correction Code (ECC) protected. Single-bit errors are corrected and can be counted under program control, while double-bit errors are detected and reported as a non-maskable interrupt (NMI) back to the 80960. Random access cycle time to the DRAM is 200 nanoseconds (ns) and page mode cycle time is 80 ns.

Note: Both the Micro Channel and PCI platforms require that packet memory be installed. The minimum size is software dependant and also may depend on available technology.

Base Read-Only Memory (ROM)

The co-processor platform supports a minimum of 128KB of Base ROM. This memory contains the 80960 initialization, power on self test (POST) for the ARTIC960 adapter, and provides for an interface to the AIB ROM for execution of AIB POST and AIB initialization. The base ROM contains the VPD (Vital Product Data) information about the ARTIC960 adapter including the adapter serial number, and provides a mechanism for the AIB to supply its VPD information.

The Base ROM has a bootstrap loader that supports a basic system unit interface for loading and executing a control program on the adapter.

The ROM used on the co-processor platform is a flash memory, which can be erased and/or written while on the adapter. To prevent accidental erasure, the co-processor platform implements a protection scheme which requires a write enable bit to be set. Once this is done, the ROM can be written.

On the IBM ARTIC960 PCI Co-Processor Platform, additional protection is provided by the use of a jumper.

Serial EPROM

The IBM ARTIC960 PCI Co-Processor Platform supports the use of a serial EPROM (erasable programmable read-only memory) to supply the PCI system with configuration data. This data is programmed prior to being installed on the base card, at the time of manufacture; it cannot be erased or programmed after this time.

Memory Controller Chip Application-Specific Integrated Circuit (ASIC)

The ARTIC 32-bit Memory Controller Chip Application-Specific Integrated Circuit (ASIC) is a VLSI device that provides the interface between an Intel 80960C series processor, a local CFE bus, and two memories. The highest performance will be achieved when the 80960 executable code, data structures, and so forth, are in instruction memory and the local bus masters are transferring data (communications packets) to and from packet memory.

The ARTIC 32-bit Memory Controller Chip ASIC provides the following:

- 0.8u (actual) Semi-Custom Array
- 2 independent DRAM controllers (up to 32MB each)
- 80960CA interface
- 32-bit CFE local bus interface
- Simultaneous data transfers between 80960 and one memory, local bus master to other memory
- Supports 3-1-1-1 memory reads, 2-1-1-1 writes
- Flow-through ECC for both DRAMs (no delay to correct an error)
- memory protection unit
- local bus arbiter
- 5 timers
- Asynchronous serial data port
- Operation at 25MHz
- 250 signals on a 15mm image in a 304 lead flat pack
- 5 Volt ± 10% operation

Performance

On the Intel 80960CA bus, the chip will support 3-1-1-1-0 cycles (36MB) to either memory. Up to 4-word bursts (quad word aligned) will be supported. The Memory Controller Chip will also support 3-1-1-1-1 reads (2-1-1-1-1 writes) from the local bus to packet memory (4-1-1-1-1 to instruction memory). However, the local bus may burst more than four words. This translates to:

- 33 MB for 4-word bursts
- 40 MB for 8-word bursts
- 44 MB for 16-word bursts

Memory Protection

The Memory Controller Chip allows for protection of the entire 80960 4GB address space. The protection scheme breaks the 80960 address space into 4 sections:

1. Low Memory (LOWMEM) accesses from 00000000h to 1FEFFFFFh
2. Upper Memory (UPMEM) accesses from 80000000h to FFFFFFFFh
3. Ram and I/O (RAMIO) accesses to DRAM and 1FFxxxxxh
4. Local Bus (LBMEM) accesses from 20000000h to 7FFFFFFFh

Limited protection for System Bus Interface Chip accesses also has been provided.

System Bus Interface Chip

The following sections show the differences between the two versions of the System Bus Interface Chip. "Micro Channel Interface Chip Application-Specific Integrated Circuit (ASIC)" describes the Micro Channel features of the chip. "PCI System Bus Interface Chip" on page 1-6 describes the PCI features of the chip.

Micro Channel Interface Chip Application-Specific Integrated Circuit (ASIC)

The major functions of the ARTIC 32-bit Micro Channel Interface Chip are as follows.

- Two Bus Master channels, addressable from the local bus
- One 128-byte intermediate data buffer per channel
- Linked List Chaining support for auto-initialization of either channel
- Support of Micro Channel basic transfers as master and slave
- Support of 64-bit, 100 ns streaming data as master and slave
- Slave write buffer (192 bytes) for better Micro Channel utilization
- Slave prefetch read buffer (32 bytes) for better Micro Channel utilization
- Hardware support for Appended I/O operations
- Hardware support for SCB Locate and Move mode
- Support of access to resident memory as both I/O and shared memory window
- Micro Channel data and address parity support
- Support for Micro Channel interrupts and error reporting
- Directly attachable to Micro Channel with 24 mA off-chip drivers
- I/O Mapping for testing of In-Circuit connections

The Micro Channel Interface Chip provides a Micro Channel slave interface, supporting 100 ns streaming data through posted memory writes and prefetched memory reads. Micro Channel Bus Masters access slave resident memory on the Local Bus through a Micro Channel shared memory window.

The Micro Channel host accesses the Local Bus through the shared memory window or through a Micro Channel I/O location.

The Micro Channel Bus Master interface consists of two Bus Master channels addressable from the Local Bus. Each channel utilizes a 128-byte intermediate buffer between resident memory and the Micro Channel. Buffering of data allows the Bus Master channel to sustain 100-ns streaming data on the Micro Channel.

Performance

The Micro Channel Interface Chip interfaces a high-speed, 80MB/sec Micro Channel interface to a high-speed Local Bus. This Local Bus is based on a 25 MHz 80960 processor bus, and has a **maximum** theoretical bandwidth of 100MB. Data rates achieved by the Micro Channel Interface Chip on the Local Bus are dependent on size of the transfer and speed of the Local Bus slave. Assuming a 64-byte burst to a zero wait state slave, the data rate is 84MB/sec. For memory or slaves requiring wait states, the data rate may be much lower.

The data rate sustained on the Micro Channel also is dependent on the speed of the Local Bus slave. With the intermediate data buffering provided internal to the Micro Channel Interface Chip, 80MB/sec can be sustained for an absolute minimum of 128 bytes.

The following table shows the maximum throughput between the Local Bus and the Micro Channel for Bus Master accesses, assuming 40 or 80MB/sec streaming data on the Micro Channel, and 50MB/sec (1 wait state) or 100MB/sec (0 wait state) Local Bus accesses.

Table 1-1. Micro Channel Interface Chip Bus Master Performance (in MB/sec)		
Micro Channel Speed	**Local Bus Speed**	**Max Throughput**
40	50	32
80	50	41
40	100	40
80	100	55

PCI System Bus Interface Chip

The major functions of the PCI System Bus Interface Chip are as follows.

- Operationally compatible with the Micro Channel System Bus Interface Chip
- Two Bus Master channels, addressable from the CFE Local Bus
- One 128-byte intermediate data buffer per channel
- Support for Posting Status from each Bus Master Channel
- Linked List Chaining support for auto-initialization of either channel
- Slave write buffer (128 bytes) for PCI Posted Write Operation
- Slave prefetch read buffer (128 bytes) for PCI Delayed Read Operation
- Master and Slave Support of PCI Bus Commands
- Hardware support for SCB Locate and Move mode
- Support of access to the CFE Local Bus address space from both PCI I/O and memory address spaces
- PCI data and address parity support
- Support for PCI interrupts and error reporting
- Directly attachable to PCI
- JTAG for testing of In-Circuit connections

The PCI System Bus Interface Chip provides a PCI target interface, supporting posted memory writes and delayed/prefetched memory reads to the CFE Local Bus address space. These accesses are mapped to a memory window on the PCI bus. A PCI master, or initiator, can access CFE Local Bus address space through this PCI slave interface. The PCI host accesses the CFE Local Bus through this memory window or through a PCI I/O location known as the Memory Data (MDATA) port. The PCI slave interface also supports a register space, mapped to both memory and I/O space on the PCI Bus.

The PCI Bus Master interface consists of two DMA, or Bus Master channels, addressable from the CFE Local Bus, or indirectly from the PCI Bus through the MDATA port. The term *Bus Master Channel* refers to these two DMA channels' interface to the PCI System Bus Interface Chip. Each channel uses a 128-byte intermediate buffer between the CFE Local Bus and the PCI Bus.

Performance

The PCI System Bus Interface Chip interfaces a synchronous, 132 MB/sec PCI interface to a high-speed local bus, known as the CFE Local Bus. The CFE Local Bus operates at 25 MHz. At 25 MHz, this bus has a *maximum* theoretical bandwidth of 100 MB/sec. Data rates achieved by the PCI System Bus Interface Chip on the CFE Local Bus are dependent on the size of the transfer and the speed of the CFE Local Bus slave. (A CFE Local Bus slave is defined as a device on the CFE Local Bus selected during the address phase of a CFE transfer). For CFE slaves requiring wait states, the data rate may be much lower.

The data rate sustained on the PCI also is dependent on the speed of the CFE Local Bus slave. With the intermediate data buffering provided internally to the PCI System Bus Interface Chip, 132 MB/sec can be sustained for an absolute minimum of 128 bytes.

The following table shows the maximum throughput between the CFE Local Bus and the PCI Bus for DMA Bus Master channel accesses. Note that the PCI System Bus Interface Chip is capable of sustaining the Maximum Burst Rate on both busses.

Table 1-2. System Bus Interface Chip Bus Master Performance (in MB/sec)	
CFE Local Bus Speed (MHz, ws)	**Throughput (MB/sec)**
25,0	100
25,1	50

Chapter 2. Co-Processor Platform Interrupt Controller Subsystem

The IBM ARTIC960 Co-Processor Platform has an FPGA that functions as the adapter's interrupt control subsystem. The general features of the interrupt controller subsystem are as follows:

- 4 encoded interrupt inputs from the System Bus Interface Chip
- 4 encoded interrupt inputs from the Memory Controller Chip
- support for both vectoring and non-vectoring AIB devices

The co-processor platform supports 80960 expanded mode interrupting. An 8-bit interrupt vector bus is provided to directly attach to the 80960. The co-processor platform interrupt controller takes the interrupt inputs and translates these into interrupt vectors that it places on the interrupt bus for interpretation by the 80960. The System Bus Interface Chip and the Memory Controller Chip will provide 4 encoded bits to the interrupt controller, which are translated into an interrupt vector. In Direct mode, the AIB will provide 8 separate bits, which the interrupt controller will translate into an interrupt vector. The AIB can use any combination of these 8 bits.

Figure 2-1 shows the interrupt flow on the co-processor platform.
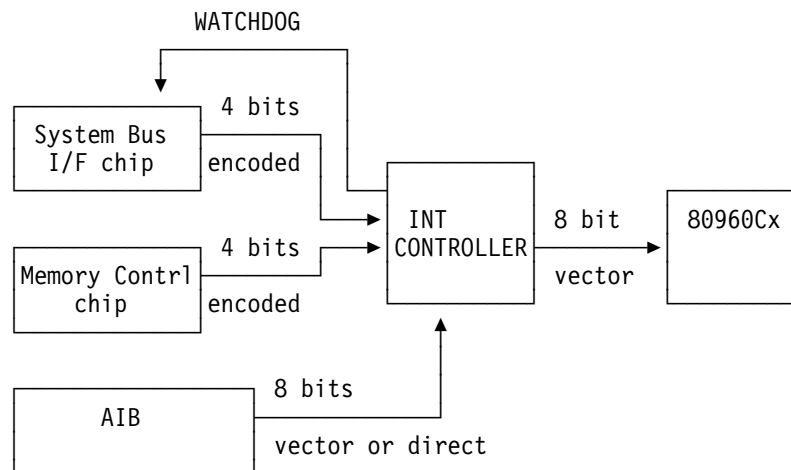
Figure   2-1. Interrupt Architecture

Support also is provided to allow AIB devices to supply the 80960 directly with an interrupt vector. This is a programmable option, and is referred to as vectored mode. The interrupt controller prioritizes the interrupts that these devices generate. The priority is fixed, with *single-bit ECC error* being the lowest and the *NMI sources* being the highest.

Interrupt inputs are not latched by the interrupt controller. The output of the interrupt controller to the 80960 interrupt bus reflects the value of the highest priority input active.

The structure and format of the Interrupt table, the vectors used by the base card and those dedicated for AIB use, are documented in "IBM ARTIC960 Co-Processor Platform Interrupt Table" on page 8-20.

Programmable Options

AIB configuration of the interrupt controller FPGA chip is required before the base card will recognize AIB interrupts. The AIB Initialization or POST code in the AIB ROM should set the AIB interrupt mode and enable interrupts.

Enable/Detect Register (EDR)

The EDR is used to select the AIB interrupt mode, which can be vectored or direct. Other bits in this register are used to indicate the presence of an AIB, and to control a light-emitting diode (LED).

Register Format

```
(80960 ADDRESS = 0A000004h) r/w  (8-Bit Access Only)

7          4 3   2    1    0

|          |INT|DCD|VCT/|LED|
| Reserved |EN |DET|-DIR|EN |
```

- Bit 7–4. Reserved.

- Bit 3. AIB INTERRUPT ENABLE. This bit is used to enable or disable interrupts from the AIB. When this bit is set to 1, interrupts are enabled. When this bit is set to 0, interrupts are disabled.

- Bit 2. AIB Detect. This bit indicates whether or not an AIB is connected to the co-processor platform. If this bit reads 1, an AIB is present.

- Bit 1. VCT/-DIR (VECTOR/-DIRECT). This bit selects the daughter card interrupt mode. When this bit is set to 1, the AIB provides an 8-bit, 80960 interrupt vector. This vector is passed through the interrupt controller to the processor. When this bit is set to 0, then each one of the 8 bits from the AIB is treated as a separate interrupt. The following figure shows the vectors associated with the eight AIB interrupt lines, when this bit is 0.

Interrupt #	Vector dec	hex
7	219	DB
6	218	DA
5	217	D9
4	216	D8
3	75	4B
2	74	4A
1	73	49
0	72	48

- Bit 0. LED enable. This bit is set to 1 to enable an external LED, and reset to 0 to disable the LED.

Reset Conditions

```
Base ROM INITIALIZATION : uuuu n-n1  - = Read Only
(prior to AIB Init/POST)             n = set by the AIB
```

Chapter 3. AIB Architecture

AIBs must conform to certain hardware and software specifications to enable reliable operation on the IBM ARTIC960 Co-Processor Platforms.

From a *hardware* perspective, the AIB must conform to the general AIB raw card form factor shown in this document. That is, the basic dimensions for the AIB, location of mounting holes, and AIB connector type must be used when developing an AIB. AIBs that adhere to the "Type-3" dimensions and are assembled with removable brackets and shields can be used on either the IBM ARTIC960 Co-Processor Platform (Micro Channel) or the IBM ARTIC960 PCI Co-Processor Platform. AIBs can be developed with dimensions larger than Type 3 in two instances. If the developer's host system (Micro Channel) supports taller adapter cards, the AIB can grow above the AIB connector. If the AIB is to be used only on the IBM ARTIC960 PCI Co-Processor Platform, it can grow below the AIB connector. See Chapter 10, "AIB Physical Characteristics" for details.

An AIB must also provide proper loading and termination of all AIB interface signals as specified by this document. AIBs must meet the AIB signal timings as specified in this manual. All AIBs are required to support AIB ROM.

From a *software* perspective, the AIB must support the minimum AIB ROM requirements as outlined by this manual. An AIB ROM must support the AIB_ROM_ANCHOR structure, and additionally can contain: AIB Post code, AIB initialization code, system unit BIOS executable code, and VPD.

Locating the AIB in the proper address regions as outlined by this manual is required to ensure operation with the IBM ARTIC960 Co-Processor Platforms software products (Kernel, Device Driver, and so forth).

A section regarding the IBM ARTIC960 Co-Processor Platforms diagnostics interface for AIBs outlines the necessary software components required to support an integrated adapter and AIB diagnostics strategy.

AIB Address Mapping

The AIB resides on both the CFE Local bus and the ROM bus. The 80960 can access the AIB on both the CFE bus and the ROM bus. The System Bus Interface Chip (SBIC) can access the AIB on the CFE bus. The AIB, as a CFE bus master, can access IBM ARTIC960 Co-Processor Platforms DRAM memory, as well as the Memory Controller Chip and SBIC CFE register sets. In fact, the AIB as a CFE bus master is capable of accessing any entity that resides on the CFE bus. Likewise, the SBIC has access to the entire CFE address space.

The following sections describe the address regions available on both the CFE and ROM buses that are available for AIB use, and the operation of the 80960 and SBIC when accessing these regions.

80960 Address Space

The 80960 microprocessor defines sixteen, 256MB address regions in its 4GB address space. The 80960 accesses to these regions are configurable as to the number of wait states, READY used to pace a transfer, and whether an access to the region is burst or non-burst, pipelined or non-pipelined. The regions are numbered 0 to 15; region 0 is defined as addresses from 0000 0000h to 0FFF FFFFh and region 15 is F000 0000h to FFFF FFFFh. The adapter's Base ROM initializes these regions through the MCON registers in the 80960.

Programming Considerations

ARTIC960 co-processor adapters EC level E32319 or later, and all ARTIC960 PCI co-processor adapters, provide hardware support for 80960CF data caching. Since the two adapters implement the caching scheme differently, memory region overlays are different on these adapters, except in both cases, region 10 will overlap region 2. This allows the Memory Controller Chip (region 2) to be accessed starting at address A000 0000h, where the data cache can be enabled. The 80960 must always be configured to the following for proper operation of the adapter.

For IBM ARTIC960 prior to EC level E32319:

- READY must be disabled for regions 0, and 8 through 15.
- BURST must be disabled for regions 0, 1, and 3 through 15.
- PIPELINE must be disabled for regions 0 through 15.

For IBM ARTIC960 EC level E32319 or later:

- READY must be disabled for regions 0, 4 through 8, and 12 through 15.
- BURST must be disabled for regions 0, 1, 3 through 9, and 11 through 15.
- PIPELINE must be disabled for regions 0 through 15.

For IBM ARTIC960 PCI:

- READY must be disabled for regions 0, 8, and 12 through 15.
- BURST must be disabled for regions 0, 1, 3 through 9, and 11 through 15.
- PIPELINE must be disabled for regions 0 through 15.

Notes:

1. Regions 0 and 15 on all IBM ARTIC960 and ARTIC960 PCI adapters, and region 8 on the IBM ARTIC960 PCI adapter, are 8-bit-wide (byte) bus regions programmed to 6 wait states from address to data, and 1 wait state for data to next address (recovery). The Base ROM and AIB ROM are located in these regions. All other Regions should be programmed to 0 wait states.

2. Although BURST is enabled in region 2, bursting is only supported to DRAM. Bursting from the 80960 is not supported to the CFE bus in any region.

The following address map defines the 80960 address space for the IBM ARTIC960 Co-Processor Platform. Within the 80960 address space, regions 1 to 7 (addresses 1000 0000h to 7FFF FFFFh) directly map onto the CFE local bus. 80960 access to all other regions do not appear on the CFE local bus. DRAM and the Memory Controller Chip registers are shared resources between the 80960 and the CFE local bus. Accesses to these shared resources do not cause cycles to appear on the CFE local bus.

From	To	Mapping	Description
			Table 3-1. IBM ARTIC960 Co-Processor Platform Address Map as Viewed by 80960
00000000	09FFFFEF	-	Reserved
09FFFFF0	0BFFFFFF	-	Base Card I/O
0C000000	0DFFFFFF	-	AIB ROM Area (AIB ROM Chip Select Active)
0E000000	0FFFFFFF	-	Base ROM Area
10000000	1FEFFFFF	CFE	Reserved
1FF00000	1FF9FFFF	CFE	AIB Register Area (Non-Burst CFE)
1FFA0000	1FFAFFFF	CFE	System Bus Interface Chip Register Set (Non-Burst CFE)
1FFB0000	1FFBFFFF	CFE	Memory Controller Chip Register Set (Non-Burst CFE)
1FFC0000	1FFFFFFF	CFE	Reserved (Non-Burst CFE)
20000000	25FFFFFF	CFE	IBM ARTIC960 Co-Processor Platform DRAM Area. In areas where DRAM is located, the 80960 accesses do not appear on the CFE bus, and the Memory Controller Chip responds to the memory access. Packet memory can be located from 20000000 up to 21FFFFFF, Instruction memory can be located from 22000000 up to 23FFFFFF. All other addresses in this region are reserved.
26000000	2FFFFFFF	CFE	AIB Memory Area
30000000	9FFFFFFF	-	Reserved
A0000000[1]	AFFFFFFF	-	Reserved Burst RAM Area. In areas where DRAM is located, the 80960 accesses do not appear on the CFE bus, and the Memory Controller Chip responds to the memory access. Packet memory can be located from A0000000 up to A1FFFFFF. Instruction memory can be located from A2000000 up to A3FFFFFF. All other addresses in this region are reserved.
B0000000	FFFFFEFF	-	Reserved
FFFFFF00	FFFFFF2F	-	Base ROM Area (80960 IBR)
FFFFFF30	FFFFFFFF	-	Reserved
1: Maps to region 2 when hardware is enabled.			

CFE Address Space

The CFE address space is broken into two separate sections: the Non-Burst section (0000 0000h – 1FFF FFFFh) and the Burst section (2000 0000 – FFFF FFFF). Bursting on the CFE bus yields a significant throughput advantage over non-bursting. See Chapter 6, "Common Front End (CFE)" for information on Bursting and Non-Bursting. In general, an AIB should locate its register set in the Non-Burst section, and locate its memory or memory-like devices in the Burst section.

Two CFE address ranges, or groups of regions, have been defined for AIB usage in both the Burst and the Non-Burst AIB regions:

- AIB Non-Bursting range (1FF00000h – 1FF9FFFFh)
- AIB Bursting range (26000000h – 2FFFFFFFh)

The AIB should allow its address space to be programmable in each of these regions. See "Reprogrammable CFE Address Space for an AIB" on page 3-9 for more details on reprogramming the AIB address space.

All other address regions in CFE address space are reserved.

The following table describes the CFE address map.

Table 3-2. IBM ARTIC960 Co-Processor Platform CFE Address Map as Viewed by an AIB			
From	**To**	**Access**	**Description**
00000000	1FEFFFFF	Non-Burst	Reserved
1FF00000	1FF9FFFF	Non-Burst	AIB Register Area
1FFA0000	1FFAFFFF	Non-Burst	System Bus Interface Chip Register Set
1FFB0000	1FFBFFFF	Non-Burst	Memory Controller Chip Register Set
1FFC0000	1FFFFFFF	Non-Burst	Reserved
20000000	25FFFFFF	Burst	IBM ARTIC960 Co-Processor Platform DRAM is located in this region
26000000	2FFFFFFF	Burst	AIB Memory Area
30000000	FFFFFFFF	Burst	Reserved

Non-Bursting, I/O Range (1FF00000h – 1FF9FFFFh)

This range is a fixed range dedicated for AIB usage. In general, an AIB should locate its memory mapped registers in this range. Note that the Memory Controller Chip memory protection scheme provides the greatest protection over the RAMIO range, which begins at 1FFxxxxxh. It is suggested that an AIB locate its register set in this address range on 4-byte boundaries. This address range is non-bursting when being accessed by the System Bus Interface Chip. Prefetching is also disabled for System Bus slave read accesses through the HSBR/MDATA access mechanism.

Bursting, Relocatable Range (26000000h – 2FFFFFFFh)

This address region above DRAM is available for AIB usage. In this region, the System Bus Interface Chip will burst, and the 80960 will not burst on the CFE bus. It is suggested that an AIB locate its memory or memory-like 32-bit devices in this range. It also is suggested that the devices in this range be located on an address boundary equal in size to the memory being located.

Within an AIB register set, it is suggested that relocation pointers be provided to allow an AIB to be relocated in the relocatable address region. For example, if an AIB has 1MB of burst contiguous memory, it may be desirable to map that memory as follows.
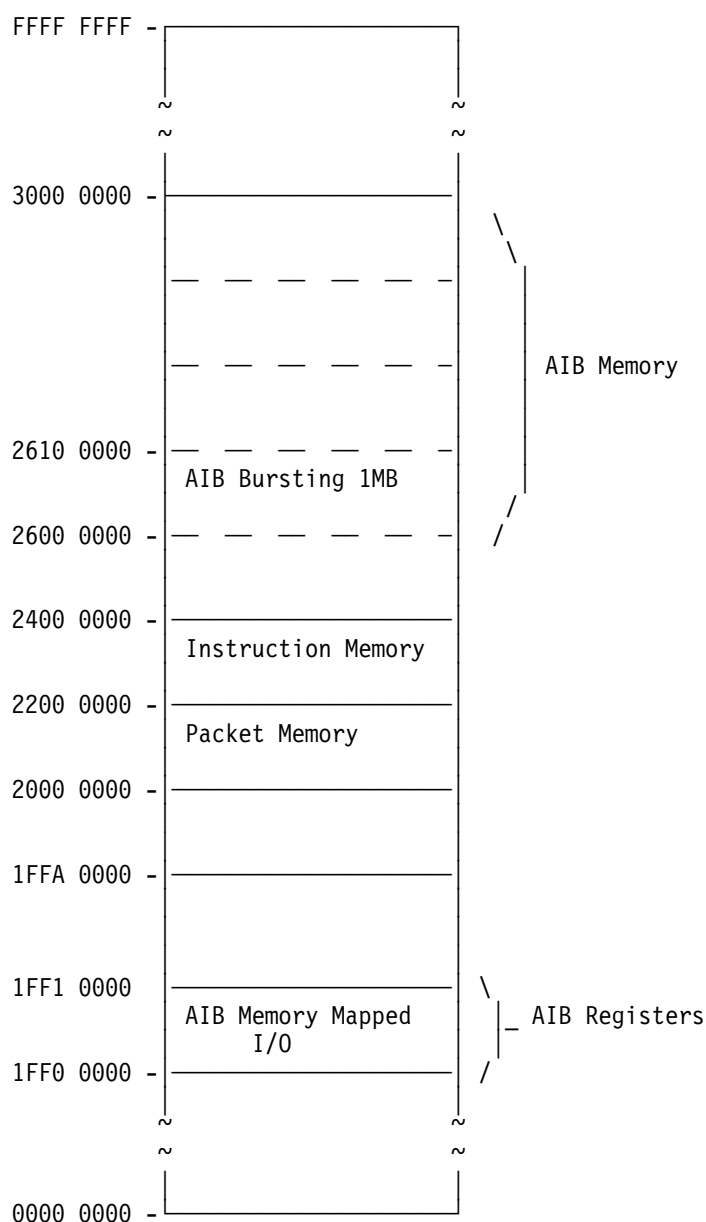
```
FFFF FFFF -  ┌─────────────────┐
             │                 │
             ~                 ~
             ~                 ~
             │                 │
3000 0000 -  ├─────────────────┤          \
             │                 │           \
             │  ─  ─  ─  ─  ─  │            \
             │                 │            │
             │  ─  ─  ─  ─  ─  │            │  AIB Memory
             │                 │            │
2610 0000 -  ├ ─  ─  ─  ─  ─  ─│            │
             │ AIB Bursting 1MB│            │
             │                 │           /│
2600 0000 -  │ ─  ─  ─  ─  ─  ─│          /
             │                 │
2400 0000 -  ├─────────────────┤
             │ Instruction Memory │
             │                 │
2200 0000 -  ├─────────────────┤
             │  Packet Memory  │
             │                 │
2000 0000 -  ├─────────────────┤
             │                 │
1FFA 0000 -  ├─────────────────┤
             │                 │
             │                 │
1FF1 0000    ├─────────────────┤    \
             │ AIB Memory Mapped│     │_  AIB Registers
             │       I/O       │     │
1FF0 0000 -  ├─────────────────┤    /
             │                 │
             ~                 ~
             ~                 ~
             │                 │
0000 0000 -  └─────────────────┘
```

Figure   3-1. AIB Address Mapping Example

In the previous example, the AIB has its register set starting at base address 1FF00000h, and its 1MB of memory located at 26000000h. A pointer register for relocating the 1MB of memory would be located somewhere in the 1FF0 xxxx range. It is suggested that the AIB CFE devices have completely reprogrammable address spaces. Reprogrammable CFE devices are discussed in "Reprogrammable CFE Address Space for an AIB" on page 3-9. Note that it is not required to have the AIB address range relocatable.

Micro Channel Access to the CFE Address Space

Shared Memory Windows

Two windows into the CFE address space are available on the Micro Channel through the Micro Channel Interface Chip. These windows allow the system unit or another Micro Channel bus master to access the CFE bus address space. The first window is 8KB or 16KB in size, and is mapped to the base of Packet memory on the adapter (CFE address 2000 0000h). The second memory window (full memory window) is set to 64MB when instruction memory is present (set to the size of Packet memory when instruction memory is not present) and also is located at the base of Packet memory (CFE address 2000 0000h). The Micro Channel addresses of these windows are configured during system unit setup by programming the Micro Channel Interface Chip POS registers. The starting location (base address) of both windows on the CFE bus is set by the base ROM during initialization of the IBM ARTIC960 Co-Processor Platform by programming the LBBAR (Local Bus Base Address Register) in the Micro Channel Interface Chip.