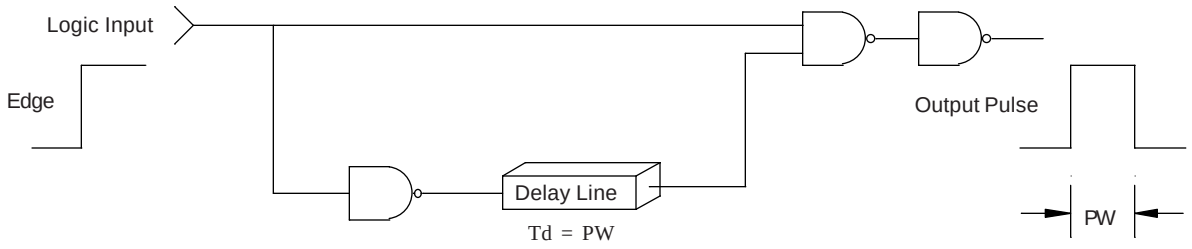
Applications

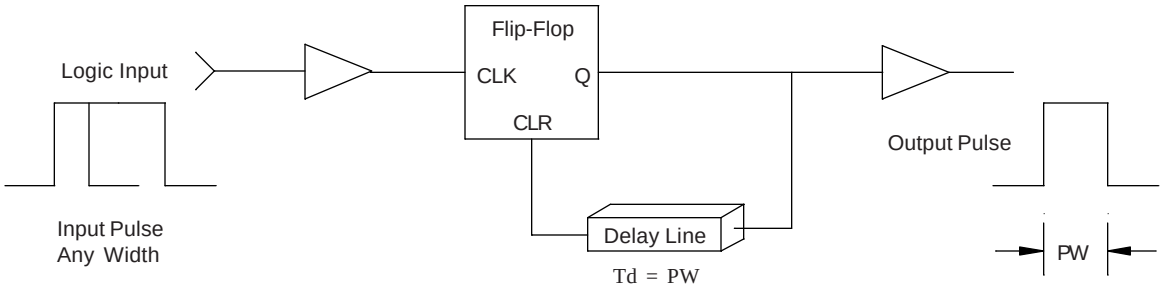
Pulse Shaping / Clock Pulse Generation Circuits

The operation and application of high speed integrated circuitry with logic propagation times in the range from 2 nsec to 20 nsec requires the conversion of logic edges to pulses. **bel**'s delay lines allow these functions to be performed in close proximity to the actual logic circuits and in the same packaging technology employed by the logic circuit set. **bel**'s Active or passive delay lines can be automatically inserted into or placed upon circuit boards along with the integrated logic circuits.

In large computer systems clock pulses are distributed to many different points within the data processing hardware over large distances. Pulse degradation due to attentuation, logic skew, spurious noise, etc. can cause intermittent systems operation. Bel's delay lines in conjunction with logic gates and/or flip-flops permit efficient means of local clock pulse regeneration. This contributes greatly to the preservation of integrity of the logic system.

The figure below shows two application methods of the use of **bel**'s delay lines for pulse shaping and clock pulse generation.





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