CL-PD6712/'20/'22

Preliminary Data Sheet

ISA–to–PC-Card Host Adapters

FEATURES

- **Single-chip PC Card host adapters**
- **Direct connection to ISA (PC AT) bus and one or two PC Card sockets**
- **Compliant with PC Card Standard, PCMCIA 2.1, and JEIDA 4.1**
- **82365SL-compatible register set, ExCA™-compatible**
- **Automatic Low-Power Dynamic mode for lowest active power consumption**
- **Programmable Suspend mode**
- **Hardware-enabled Super Suspend mode**
- **Five programmable memory windows per socket and two programmable I/O windows per socket**
- **Programmable card access cycle timing**
- **8- or 16-bit system bus interface**
- **8- and 16-bit PC Card interface support**
- **ATA disk interface support**
- **DMA support (CL-PD6712 and CL-PD6722)**
- **Card-voltage sense support**
- **PC Card activity indicator**
- **Mixed-voltage operation (3.3/5.0 V)**
- **Single-socket interface: 144-pin VQFP for smallest form factor (CL-PD6712)**
- **Dual-socket interface: 208-pin PQFP or VQFP (CL-PD6720 and CL-PD6722)**

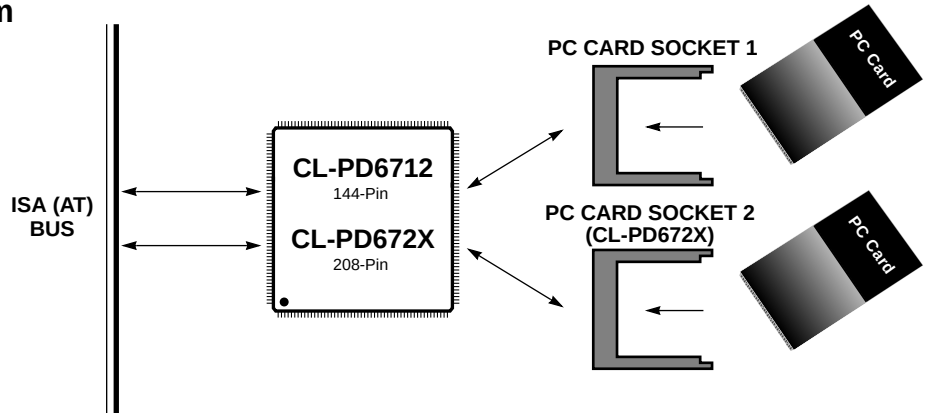
OVERVIEW

The CL-PD6712, CL-PD6720, and CL-PD6722 are single-chip PC Card host adapter solutions capable of controlling one (CL-PD6712) or two (CL-PD6720 and CL-PD6722) PC Card sockets. The chips are compliant with PC Card Standard, PCMCIA 2.1, and JEIDA 4.1 and are optimized for use in notebook and handheld computers where reduced form factor and low power consumption are critical design objectives. With the CL-PD6712, a complete PC Card solution with power-control logic can occupy less than 1.5 square inches (excluding the socket connector). With the CL-PD6720 or CL-PD6722, a complete dual-socket PC Card solution with power-control logic can occupy less than 2 square inches (excluding socket connectors).

The chips employ energy-efficient mixed-voltage technology that can reduce system power consumption by over 50 percent. The chips also provide: a Low-Power Dynamic mode, which automatically stops the internal clock during periods of card inactivity; a software-controlled Suspend mode, which dramatically reduces power by disabling most of the internal circuitry and stopping data transactions to the

(cont.)

System Block Diagram



OVERVIEW (cont.)

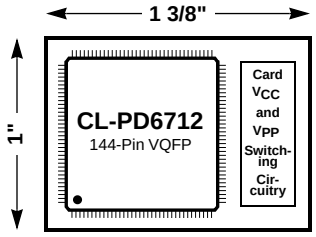
PC Cards; and a hardware-controlled Super Suspend mode, which reduces current to the µA range.

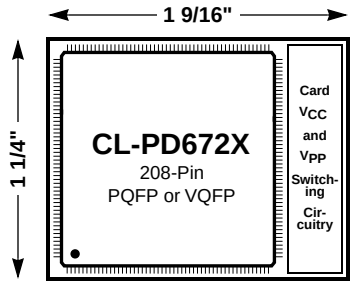
Personal computer applications typically access PC Cards through a third-party socket/card-services software interface. To assure full compatibility with industry-standard socket/card-services software and PC Card applications, the register set in the CL-PD6712 and CL-PD672X is a superset of the Intel® 82365SL register set.

The chips provide fully buffered PC Card interfaces, meaning that no external logic is required for buffering signals to/from the interface, and power consumption can be controlled by limiting signal transitions on the PC Card bus.

Notebook Computer Design Priorities	*Supporting Features*
■ Small Form Factor	❒ Single-chip solutions ❒ No external buffers for host or socket ❒ Efficient board layout
■ Minimum Power Consumption	❒ Automatic Low-Power Dynamic mode ❒ Hardware- and software-controlled Suspend modes ❒ Mixed-voltage operation
■ High Performance	❒ Write cache ❒ Programmable timing supports more cards, faster reads and writes ❒ Automatic bus sizing for 8- or 16-bit ❒ DMA available with the CL-PD6712 and CL-PD6722
■ Compatibility	❒ Compliant with PC Card Standard, PCMCIA 2.1, and JEIDA 4.1 ❒ 82365SL A-step register-compatible, ExCA™-compatible

Host Adapter Form Factor





For the CL-PD6720, this data sheet applies to Revision D and above. For data on an earlier revision of the CL-PD6720, please use Version 2.5 of the CL-PD6710/PD672X Data Sheet.

Table of Contents

Document Revision History

Version 3.0

Following are major changes between July 1994 and September 1995 versions of this data sheet:

General

A new chip was added: the CL-PD6712, which replaces the CL-PD6710.

Extended register set was expanded.

208-pin VQFP package option was added for the CL-PD6720 and CL-PD6722.

Some windowing register names were changed to specify either card or system.

References to PCMCIA card were changed to PC Card.

The chips are compatible with PC Card Standard, as R2 PC Card controllers.

For the CL-PD6712, two pin names are different than the CL-PD6710 to reflect new functionality:

5V_DET became VS1#/A_GPSTB
N.C./RESERVED became VS2#/B_GPSTB

For the CL-PD672X, two pin names were changed to reflect new functionality:

A_5V_DET became A_GPSTB
B_5V_DET became B_GPSTB

For the CL-PD67XX, four pin names were changed to reflect their full functionality:

IRQ12 became IRQ12/LED_OUT*
IRQ15 became IRQ15/RI_OUT*
BVD1/-STSCHG became BVD1/-STSCHG/-RI
BVD2/-SPKR became BVD2/-SPKR/-LED

For the CL-PD67XX, two pin names were changed to match other Cirrus Logic PC Card products:

SLOT_VCC became SOCKET_VCC
VDD became CORE_VDD

Section

2.2 I/O type codes changed.

2.3 Table columns rearranged, power control pins placed in their own table.

Table added for general-purpose strobe / voltage sense pins.

3.1.2 Windowing figures added.

3.1.3 Functional block figure added.

3.1.5 More information about LED_OUT*, RI_OUT*, DACK*, and DRQ alternate functions of interrupt pins added.

3.1.6 Section on general-purpose strobe added.

3.1.7 Section on voltage sense added.

3.2 Sample code for accessing registers added.

4 Read/Write Convention table added.

6.3 Auto-Power bit description changed.

6.4 IRQ Level bits name changed to Card IRQ Select.

6.6 Management IRQ bits name changed to Management IRQ Select.

9.1 5V Detect (bit 0 of index 16h) is now Reserved.

9.4 Chip Identification (bits 7:6 of index 1Fh) is now named Cirrus Logic Host-Adapter Identification.

9.7 **External Data** and **Extension Control 2** registers added.

LED Activity Enable bit added to **Extension Control 1** register. Auto Power Clear bit name changed to Auto Power Clear Disable.

10 '11' value of Prescalar Select bits of timing registers changed to 8192.

For Command Multiplier Value bits, order of reset states for Timing sets 0 and 1 switched to show reset state for Timing set 0 first.

Recovery Timing register reset value changed to 03h to allow additional I/O cycle recovery time of systems using 'DX/4 processors.

11 ATA information is now in an application note.

12 General-purpose strobe chapter added.

13 Voltage sense chapter added.

15.1 Allowable voltage on any pin increased to ±0.5 V greater than voltage of +5V pin.

15.3 Table 15-7: values for t2, t2a, t10, t13, and t18 of ISA bus timing table changed.

Table 15-9: Pulse mode interrupt timing added.

Table 15-10: General-purpose strobe timing added.

Table 15-12: values of t5 and t6 of memory read/write timing table changed.

Table 15-13: -WAIT timing values added to word I/O read/write timing.

Table 15-17 and 15-18: DMA read and write cycle timing tables expanded.

16 208-pin VQFP package added.

Version 2.5

Following are major changes between October 1993 and July 1994 versions of this data sheet:

General

An extension register and two bits have been added to the CL-PD6722 register set.

Section

1.2 Description for bits labeled Reserved, Compatibility, 0 or 1, and Scratchpad have been clarified.

5.2 In the table for "Bits 1-0: Battery Voltage Detect", the column headings for bit 1 and bit 0 were reversed, and have been corrected.

5–7 Bits 6, 3, and 2 (index 2h), bits 6 and 2 (index 7h), and bit 6 (index 11h, 19h, 21h, 29h, 31h) have been relabeled Compatibility bits.

6.6 Bit 0 (index 36h, 38h) has been relabeled *0.*

8.4 Bit 1 (index 1Fh) has been changed to be a part of the CL-PD67XX Revision Level field. Bit 0 has been relabeled Reserved.

8.7 Two bits, Auto-Power Clear and V_{CC} Power Lock, and a register, **Maximum DMA Acknowledge Delay**, have been added to descriptions of the CL-PD6722 registers. The **DMA Control** register was renamed **Extension Control 1**. The Disable Socket Pull-Ups bit was renamed Pull-Up Control.

11.3 References to -WE and -OE in the last paragraph have been corrected.

11.4.1 The table on DMA signal usage and Figure 11-2 have been slightly modified.

13 The 144- and 208-pin package drawings have been updated.

Version 2

Following are major changes between January 1993 and October 1993 versions of this data sheet:

General

A new chip was added: the CL-PD6722.

The CL-PD672X packaging name was changed to PQFP; the physical package is the same.

The chips are also compatible with PCMCIA 2.1.

Section

2.2 SPKR_OUT*/CSEL pin description in Table 2-1 was changed from TO-PU type to IO-PU type.

Addition of the CL-PD6722 chip changed description in Tables 2-1 and 2-2 of the following pins: IRQ9, IRQ10, -VPP_VALID, -REG, -OE, -WE, WP/-IOIS16, -INPACK, and BVD2/-SPKR.

3.1 The typical power consumption values in Table 3-1 were updated (reduced) to more closely reflect expected values.

Sections 3.1.10 and 3.1.11 are new sections describing the CL-PD6722.

5–9 Many indications of Constant bits in registers were changed from "0" to "Scratch Bit".

5 In the Card Status Change register, the Battery Dead/STSCHG Enable bit name was renamed Battery Dead Or Status Change Enable.

8 The Misc Control 2 register bit 6 is not reserved on the CL-PD6722. Its functionality is described.

Sections 8.6 and 8.7 were added to describe CL-PD6722–specific registers.

9 The Setup, Command, and Recovery field names were altered. The default state for the Command Multiplier Value field was corrected. The timing formulas for all three timing register sets were reformatted. The timing with '11' values selected on the Prescalar Select field will calculate differently.

11 This new chapter describes DMA on the CL-PD6722.

12 Extensive changes were made throughout this chapter. Please review carefully.

1. GENERAL CONVENTIONS

The following general conventions apply to this document.

Throughout this document, *CL-PD67XX* means CL-PD6712, CL-PD6720, and CL-PD6722. Likewise, *CL-PD672X* means CL-PD6720 and CL-PD6722.

Bits within words and words within various memory spaces are generally numbered with a *0* (zero) as the least-significant bit or word. For example, the least-significant bit of a byte is bit 0, while the most-significant bit is bit 7.

In addition, number ranges for bit fields and words are presented with the most-significant value first. Thus, when discussing a bit field within a register, the bit number of the most-significant bit is written first, followed by a colon (:) and then the bit number of the least-significant bit; as in, bits 7:0.

In this document, the names of the CL-PD67XX internal registers are bold-faced. For example, **Chip Revision** and **Power Control** are register names. The names of bit fields are written with initial uppercase letters. For example, Card Power On and Battery Voltage Detect are bit field names.

Numbers and Units

The unit *Kbyte* designates 1024 bytes (2^{10}). The unit *Mbyte* designates 1,048,576 bytes (2^{20}). The unit *Gbyte* designates 1,073,741,824 bytes (2^{30}). The unit *Hz* designates hertz. The unit *kHz* designates 1000 hertz. The unit *MHz* designates 1,000,000 Hz. The unit *ms* designates millisecond. The unit *µs* designates microsecond. The unit *ns* designates nanosecond. The unit *mA* designates milliampere. The unit *V* immediately following a number designates volt.

Hexadecimal numbers are presented with all letters in uppercase and a lowercase *h* appended. For example, *14h* and *03CAh* are hexadecimal numbers.

Binary numbers are enclosed in single quotation marks when in text. For example, *'11'* is a binary number.

Numbers not indicated by an *h* or single quotation marks are decimal.

In addition, a capital letter *X* is used within numbers to indicate digits ignored by the CL-PD67XX within the current context. For example, *'101XX01'* is a binary number with bits 3:2 ignored.

2. PIN INFORMATION

The CL-PD6712 is available in a 144-pin VQFP (very tight-pitch quad flat pack) component package and the CL-PD6720 and CL-PD6722 are available in either a 208-pin PQFP (plastic quad flat pack) component package or a 208-pin VQFP component package. The interface pins can be divided into five groups:

- ISA bus interface pins
- PC Card socket interface pins (one or two sets)
- General-purpose strobe / voltage sense pins
- Power control pins
- Power and ground pins

Refer to Figure 2-1 for the CL-PD6712 and Figure 2-2 for the CL-PD6720 and CL-PD6722 pin diagrams. The pin assignments for the groups of interface pins are shown in Table 2-1 through Table 2-5.

2.1 Pin Diagrams

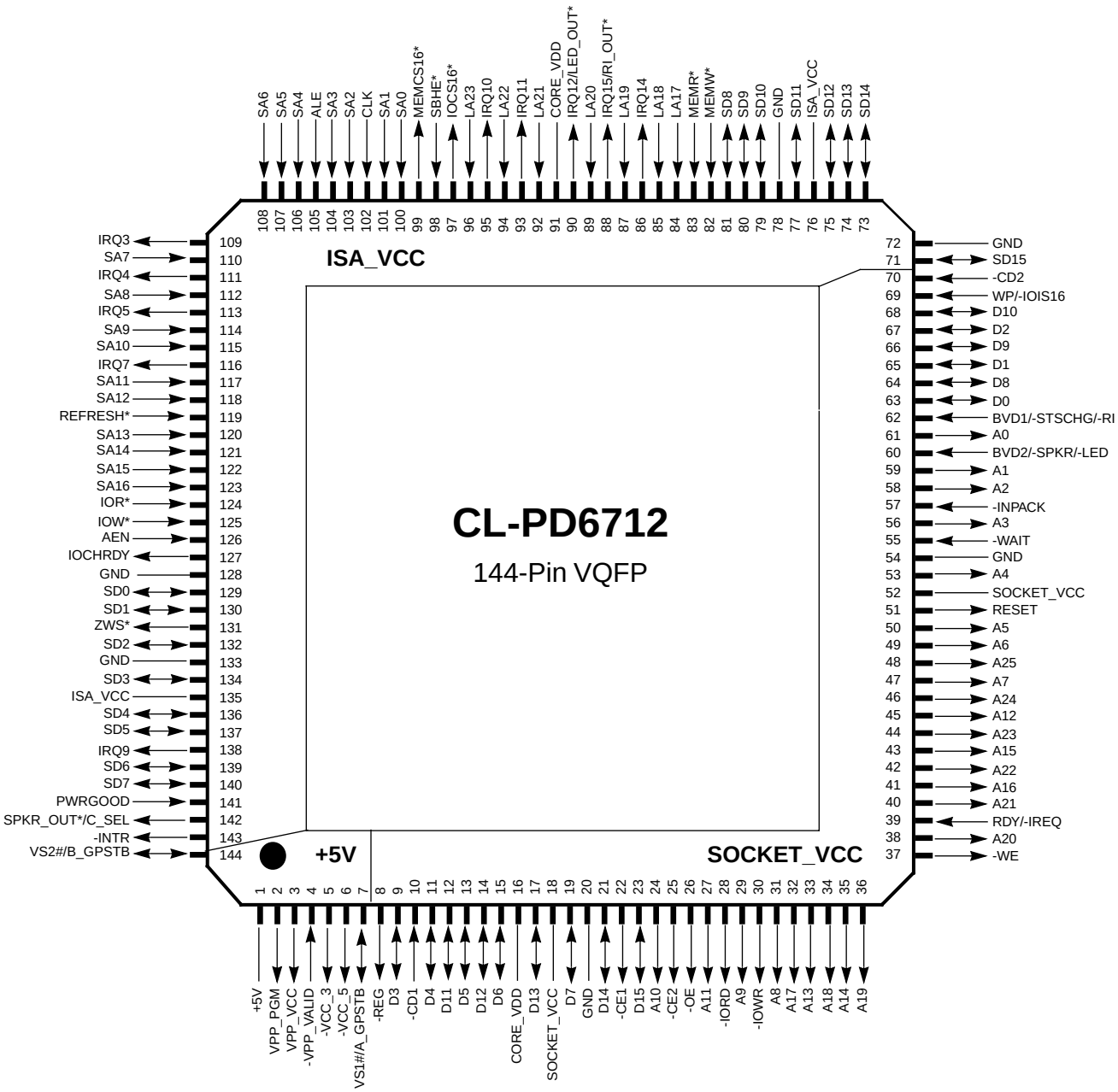


Figure 2-1. CL-PD6712 Pin Diagram

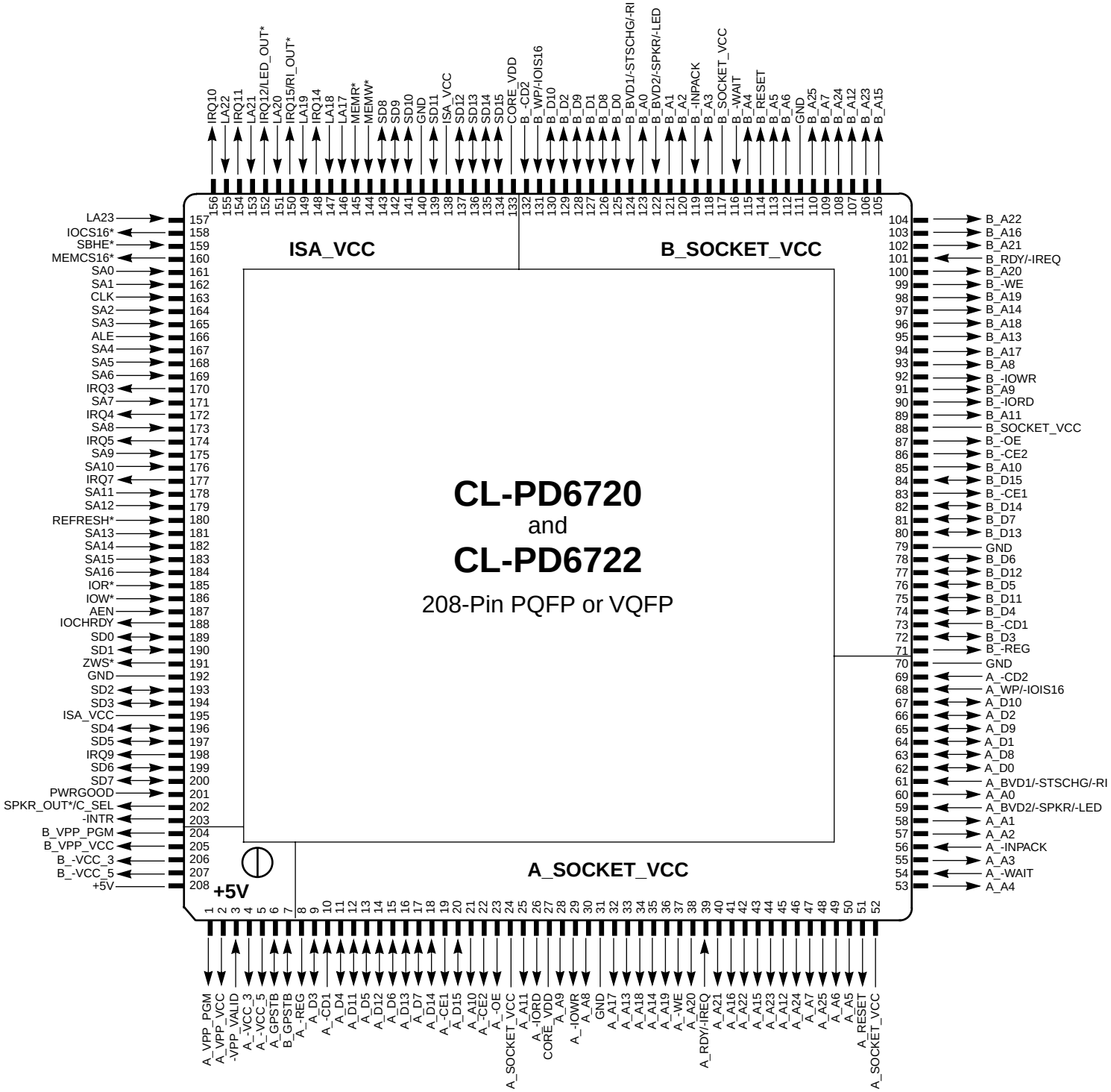


Figure 2-2. CL-PD6720 and CL-PD6722 Pin Diagram

2.2 Pin Description Conventions

The following conventions apply to the pin description tables in Section 2.3:

- A dash (-) at the beginning of a pin name indicates an active-low signal for the PC Card bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal for the ISA bus or that is a general-interface for the CL-PD67XX.
- Pins marked with a dagger (†) in the pin description tables can be switched between CMOS and TTL input levels when CORE_VDD is powered at 5 volts. All other pins use CMOS input levels when CORE_VDD is powered at 5 volts and TTL input levels when powered at 3.3 volts.
- A pin name ending in bracketed digits separated by a colon [n:n] indicates a multi-pin bus.
- The pin number (Pin Number) column indicates the package pin that carries the listed signal. Note that multi-pin buses are listed with the first pin number corresponding to the most-significant bit of the bus. For example, pin numbers 123:120, 118, 117, 115, 114, 112, 110, 108:106, 104, 103, 101, and 100 are associated with ISA Bus Address Input and Data Input/Output pins SA[16:0] and indicate that:
  - SA16 is pin 123
  - SA15 is pin 122
  - SA0 is pin 100
- The quantity (Qty.) column indicates the number of pins used (per socket where applicable).
- The I/O-type code (I/O) column indicates the input and output configurations of the pins on the CL-PD67XX.The possible types are defined below.
- The power-type code (Pwr.) column indicates the output drive power source for an output pin or the pull-up power source for an input pin on the CL-PD67XX. The possible types are defined below.

I/O Type	Description
I	Input pin
O	Constant-driven output pin
I/O	Input/output pin
O-OD	Open-drain output pin
O-TS	Tristate output pin
-PU	An internal pull-up resistor is present
GND	Ground pin
PWR	Power pin

Power Type	Output or Pull-up Power Source
1	+5V: powered from a 5.0-volt power supply in most systems (see description of +5V pin in Table 2-5)
2	A_SOCKET_VCC: powered from the Socket A V_{CC} supply connecting to PC Card pins 17 and 51 of Socket A
3	B_SOCKET_VCC: powered from the Socket B V_{CC} supply connecting to PC Card pins 17 and 51 of Socket B
4	ISA_VCC: powered from the ISA bus power supply
5	CORE_VDD: usually powered from the lowest available power supply for lowest power consumption, which in most systems is 3.3 volts

NOTE: All pin inputs are referenced to CORE_VDD, independent of their output supply voltage.

- The drive-type (Drive) column describes the output drive-type of the pin (see DC specifications in Chapter 15 for more information). Note that the drive type listed for an input-only (I) pin is not applicable (–).

2.3 Pin Descriptions

Table 2-1. ISA Bus Interface Pins

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/ CL-PD6722				
LA[23:17]	**ISA Bus Address Input**: Connect to ISA signals LA[23:17] or, for systems limited to 1-Mbyte address space, tie ALE high, ground LA[23:20] and connect LA[19:17] to ISA signals SA[19:17].	96, 94, 92, 89, 87, 85, 84	157, 155, 153, 151, 149, 147, 146	7	I	4	–
SA[16:0]	**ISA Bus Address Input**: Connect to ISA signals SA[16:0].	123:120, 118, 117, 115, 114, 112, 110, 108:106, 104, 103, 101, 100	184:181, 179, 178, 176, 175, 173, 171, 169:167, 165, 164, 162, 161	17	I	4	–
SD[15:0]	**ISA Bus Data Input/Output**: These pins are used to transfer data during a memory or I/O cycle. Connect to ISA signals SD[15:0]. For 8-bit system buses, leave SD[15:8] unconnected.	71, 73–75, 77, 79–81, 140, 139, 137, 136, 134, 132, 130, 129	134–137, 139, 141–143, 200, 199, 197, 196, 194, 193, 190, 189	16	I/O	4	12 mA
SBHE*	**Byte High Enable**: This input is used in conjunction with SA[0] to specify the width and alignment of a data transfer. Connect to ISA signal SBHE*. For 8-bit system buses, pull up connect to ISA_VCC supply.	98	159	1	I	4	–
IOR*	**I/O Read**: This input indicates that a host I/O read cycle is occurring. Connect to ISA signal IOR*.	124	185	1	I	4	–
IOW*	**I/O Write**: This input indicates that a host I/O write cycle is occurring. Connect to ISA signal IOW*.	125	186	1	I	4	–
MEMR*	**Memory Read**: This input indicates that a host memory read cycle is occurring. Connect to ISA signal MEMR*.	83	145	1	I	4	–
MEMW*	**Memory Write**: This input indicates that a host memory write cycle is occurring. Connect to ISA signal MEMW*.	82	144	1	I	4	–
REFRESH*	**Refresh**: This input indicates a memory refresh cycle is occurring and will cause the CL-PD67XX to ignore memory accesses on the bus. Connect to ISA signal REFRESH*.	119	180	1	I	4	–
ALE	**Address Latch Enable**: A high on this input indicates a valid memory address on the LA[23:17] bus lines. Connect to ISA signal BALE.	105	166	1	I	4	–

Table 2-1. ISA Bus Interface Pins *(cont.)*

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/ CL-PD6722				
PWRGOOD	**Power Good**: The CL-PD67XX will be reset when the POWERGOOD input is low. Connect to the POWERGOOD signal from the system power supply; or, if not available, connect to inverted RESETDRV signal from ISA bus.	141	201	1	I	4	–
AEN	**Address Enable**: This is an input from the host CPU bus signal that distinguishes between DMA and non-DMA bus cycles. This input should be high for a DMA cycle and will cause the CL-PD67XX to ignore IOR* and IOW* except when a CL-PD6712 or CL-PD6722 is configured for DMA and its DREQ (IRQ10) and DACK* (IRQ9) signals are active. Connect to ISA signal AEN. When CL-PD67XX is in Suspend mode (see Misc Control 2, bit 2 on page 61), pull this input high during system power-down for lowest power consumption.	126	187	1	I	4	–
MEMCS16*	**Memory Select 16**: This output is an acknowledge of 16-bit-wide access support and is generated by the CL-PD67XX when a valid 16-bit-word-accessible memory address has been decoded. Connect to ISA signal MEMCS16*.	99	160	1	O-OD	4	16 mA
IOCS16*	**I/O Select 16**: This output is an acknowledge for 16-bit-wide access support and is generated by the CL-PD67XX when a valid 16-bit word accessible I/O address has been decoded. Connect to ISA signal IOCS16*.	97	158	1	O-OD	4	16 mA
IOCHRDY	**I/O Channel Ready**: This output is driven low by the CL-PD67XX to lengthen host cycles. Connect to the ISA bus IOCHRDY signal.	127	188	1	O-TS	4	16 mA
IRQ[14, 11, 7, 5:3]	**Interrupt Request**: These outputs indicate programmable interrupt requests generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD67XX to the system, a common use is to connect these pins to the corresponding ISA signal names in the system.	86, 93, 116, 113, 111, 109	148, 154, 177, 174, 172, 170	6	O-TS	4	2 mA
IRQ9	**Interrupt Request 9**: In default mode this output indicates an interrupt request from one of the cards. When the CL-PD6712 or CL-PD6722 is in DMA mode (see Misc Control 2, bit 6), IRQ9 becomes an input and is connected to the ISA bus DACK* line corresponding to the ISA bus DREQ line that the IRQ10 pin is connected to. In DMA mode this signal is active-low.	138	198	1	I/O-TS	4	2 mA

Table 2-1. ISA Bus Interface Pins *(cont.)*

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/ CL-PD6722				
IRQ10	**Interrupt Request 10:** In IRQ mode this output indicates an interrupt request from one of the cards. When the CL-PD6712 or CL-PD6722 is in DMA mode (see **Misc Control 2**, bit 6), IRQ10 is the DREQ to be connected to DREQ0, 1, 2, 3, 5, 6, 7 of the ISA bus. In DMA mode this signal is active-high.	95	156	1	O-TS	4	2 mA
IRQ12/ LED_OUT*	**Interrupt Request 12 / LED Output**: In default IRQ mode this output indicates an interrupt request from one of the cards, and is connected to the ISA bus IRQ12 signal. When the Drive LED Enable bit (see page 61) is set, this output becomes an open-drain driver for a disk-active LED (see **ATA Control** register bit 1) or PC Card activity LED (see **Extension Control 1** register bit 2).	90	152	1	O-TS or O-OD	4	12 mA
IRQ15/ RI_OUT*	**Interrupt Request 15 / Ring Indicate Output**: In IRQ mode this output indicates an interrupt request from one of the cards. When the IRQ15/RI_OUT* Is RI Out bit (see page 62) is set to '1', this output is the -RI signal from the corresponding PC Card.	88	150	1	O-TS	4	2 mA
-INTR	**Interrupt**: This output indicates a management interrupt. This should be connected to the system processor's SMI or NMI interrupt input, depending on the type of processor used.	143	203	1	O-TS	4	2 mA
ZWS*	**Zero Wait State**: This output is connected to the ISA ZWS (0WS) signal. It is driven low by the CL-PD67XX when it is able to complete the current memory access cycle in zero wait states.	131	191	1	O-OD	4	16 mA

Table 2-1. ISA Bus Interface Pins *(cont.)*

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/ CL-PD6722				
SPKR_OUT*/ C_SEL	**Speaker Out / Chip Select**: This I/O pin can be used as a digital output to a speaker to allow a system to support a PC Card's -SPKR pin for fax/modem/voice and audio. During reset this pin also serves as a chip-configuration input. If the level on this pin is low when PWRGOOD rises, the CL-PD6712 is configured to support cards as a PC Card Socket 2 device, and the CL-PD672X is configured to support cards as PC Card Socket 2 and Socket 3 devices. If the level on this pin is high when PWRGOOD rises, the CL-PD6712 is configured to support cards as a PC Card Socket 0 device, and the CL-PD672X is configured to support cards as PC Card Socket 0 and Socket 1 devices. This pin is internally pulled up during reset so that default configuration of the chip as a Socket 0 (and Socket 1 for CL-PD672X) is facilitated. Adhere to the minimum pulse-width timing specification for PWRGOOD to allow the internal pull-up to operate and ensure the default configuration. Refer to the Socket Index field on page 33 for more information on chip configuration. After reset operations have completed, this pin defaults to high-impedance, and can then be enabled as a totem-pole speaker output by the setting of a card socket's Speaker Enable bit (**Misc Control 1** register, bit 4). This output then becomes the negative polarity XOR of each socket's BVD2/-SPKR/-LED input that has its Speaker Enable bit set. Refer to the Section 5.1 description of socket index values for more details.	142	202	1	I/O-PU	4	12 mA
CLK	**Clock:** This input is connected to the ISA bus OSC signal. A 14.318-MHz signal is used to derive the internal 25-MHz clock used for all socket timing. Alternately, a 25-MHz clock source can be directly connected and the internal synthesizer bypassed.	102	163	1	I	4	–
-VPP_VALID	In default mode this is a status input that can be used by software as an indication that the V_{PP} power supply is stable. When the CL-PD6712 or CL-PD6722 is in DMA mode (see Misc Control 2, bit 6), this input is connected to the TC (Terminal Count) signal of the ISA bus. In DMA mode, this signal is active-high.	4	3	1	I	1	–
ISA_VCC	**System Bus V_{CC}:** This supply pin can be set to 3.3 or 5.0 V. The ISA Bus Interface pin group (this table) operates at the voltage applied to this pin independent of the voltage applied to other pin groups.	76, 135	138, 195	2	PWR	–	–

Table 2-2. Socket Interface Pins

Pin Name[1]	Description[2]	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
-REG	**Register Access:** In Memory Card Interface mode, this output chooses between attribute and common memory. In I/O Card Interface mode for non-DMA transfers, this signal is active (low). For DMA cycles on the CL-PD6712 or CL-PD6722 to a DMA-capable card, -REG is inactive during I/O cycles to indicate a DMA cycle to or from the PC Card. In ATA mode, this signal is always inactive.	8	8	71	1	O-TS	2 or 3	2 mA
A[25:0]	PC Card socket address outputs.	48, 46, 44, 42, 40, 38, 36, 34, 32, 41, 43, 35, 33, 45, 27, 24, 29, 31, 47, 49, 50, 53, 56, 58, 59, 61	48, 46, 44, 42, 40, 38, 36, 34, 32, 41, 43, 35, 33, 45, 25, 21, 28, 30, 47, 49, 50, 53, 55, 57, 58, 60	110, 108, 106, 104, 102, 100, 98, 96, 94, 103, 105, 97, 95, 107, 89, 85, 91, 93, 109, 112, 113, 115, 118, 120, 121, 123	26	O-TS	2 or 3	2 mA
D[15:0] †	PC Card socket data I/O signals.	23, 21, 17, 14, 12, 68, 66, 64, 19, 15, 13, 11, 9, 67, 65, 63	20, 18, 16, 14, 12, 67, 65, 63, 17, 15, 13, 11, 9, 66, 64, 62	84, 82, 80, 77, 75, 130, 128, 126, 81, 78, 76, 74, 72, 129, 127, 125	16	I/O	2 or 3	2 mA
-OE	**Output Enable**: For non-DMA transfers, this output goes active (low) to indicate a memory read from the socket. During a DMA write (when -IORD is active) this output goes low if the ISA output TC is active (high), indicating to the card that the system's terminal count signal is active. During DMA reads (when -IOWR is active), this output remains high.	26	23	87	1	O-TS	2 or 3	2 mA

[1] To differentiate the sockets, all CL-PD6720 and CL-PD6722 pin names have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Table 11-1 on page 75.

Table 2-2. Socket Interface Pins *(cont.)*

Pin Name[1]	Description[2]	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
-WE	**Write Enable**: For non-DMA transfers, this signal goes active (low) to indicate a memory write to the socket. During a DMA read (when -IOWR is active), this signal goes low if the ISA output TC is active (high), indicating to the card that the system's terminal count signal is active. During DMA writes (when -IORD is active), this output remains high.	37	37	99	1	O-TS	2 or 3	2 mA
-IORD	**I/O Read**: This output is driven low for I/O reads from the socket.	28	26	90	1	O-TS	2 or 3	2 mA
-IOWR	**I/O Write**: This output is driven low for I/O writes to the socket.	30	29	92	1	O-TS	2 or 3	2 mA
WP/ -IOIS16 †	**Write Protect / I/O Is 16-Bit**: In Memory Card Interface mode (Interrupt and General Control register, bit 5 is equal to '0'), this input is the status of the PC card write protect switch. In I/O Card Interface mode, a low on this input indicates that the I/O address being accessed is capable of 16-bit operation. In DMA mode, this pin can be programmed as the -DREQ input from a DMA-capable PC Card.	69	68	131	1	I-PU	2 or 3	–
-INPACK †	**Input Acknowledge**: This input indicates to the CL-PD67XX that the PC Card supports I/O access at the current address. A PC Card activates this input during IORD cycles to which the card can respond. In DMA mode, this pin can be programmed as the -DREQ input from a DMA-capable PC Card.	57	56	119	1	I-PU	2 or 3	–
RDY/ -IREQ †	**Ready / Interrupt Request**: In Memory Card Interface mode, this input is readable as the status of bit 5 of the **Interface Status** register, which is used by a PC Card to signal system software of its ready or busy state. In I/O Card Interface mode, this active-low input indicates an interrupt request.	39	39	101	1	I-PU	2 or 3	–

[1] To differentiate the sockets, all CL-PD6720 and CL-PD6722 pin names have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Table 11-1 on page 75.

Table 2-2. Socket Interface Pins *(cont.)*

Pin Name[1]	Description[2]	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
-WAIT †	**Wait**: This input indicates to the CL-PD67XX that the current card access cycle is to be extended until this signal becomes inactive (high).	55	54	116	1	I-PU	2 or 3	–
-CD[2:1]	**Card Detect**: These inputs indicate to the CL-PD67XX the presence of a card in the socket. They are pulled high internally in the chip.	70, 10	69, 10	132, 73	2	I-PU	1	–
-CE[2:1]	**Card Enable**: These outputs are driven low by the CL-PD67XX during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 will be active and A0 will be set to '1' for odd-byte accesses.	25, 22	22, 19	86, 83	2	O-TS	2 or 3	2 mA
RESET	**Reset**: This output will be high to reset the card and low for normal operation. To reduce power consumption of idle cards and to prevent reset glitches to a card, this signal is high-impedance unless a card is fully seated in the socket and card interface signals are enabled.	51	51	114	1	O-TS	2 or 3	2 mA
BVD2/ -SPKR/ -LED †	**Battery Voltage Detect 2 / Speaker / LED**: In Memory Card Interface mode, this input serves as the BVD2 or battery warning status input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For disk-drive support, BVD2/-SPKR/-LED can also be configured as a drive-status LED input. In DMA mode, this pin can be programmed as the -DREQ input from a DMA-capable PC Card.	60	59	122	1	I-PU	2 or 3	–
BVD1/ -STSCHG/ -RI †	**Battery Voltage Detect 1 / Status Change / Ring Indicate**: In Memory Card Interface mode, this input serves as BVD1 (Battery Dead Status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the CL-PD67XX that the card's internal status has changed. In I/O Card Interface mode, this input can alternately be used as -RI ring indicate when IRQ15/RI_OUT* is configured for RI Out (see page 62).	62	61	124	1	I-PU	2 or 3	–

[1] To differentiate the sockets, all CL-PD6720 and CL-PD6722 pin names have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Table 11-1 on page 75.

Table 2-2. Socket Interface Pins *(cont.)*

Pin Name[1]	Description[2]	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
SOCKET_ VCC	Connect these pins to the V_{CC} supply of the socket (pins 17 and 51 of the respective PC Card socket). These pins can thus be 0, 3.3, or 5 V, depending on card presence, card type, and system configuration. The socket interface outputs (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD67XX pin groups.	18, 52	24, 52	88, 117	2	PWR	–	–

[1] To differentiate the sockets, all CL-PD6720 and CL-PD6722 pin names have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Table 11-1 on page 75.

Table 2-3. General-Purpose Strobe / Voltage Sense Pins

Pin Name	Description	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
VS1#/ A_GPSTB	**Voltage Sense 1 / General-Purpose Strobe A:** Connect to pin 43 on PC Card socket, or use as a general-purpose input port strobe to sense VS1 and VS2 through external hardware along with other external inputs.[a] [b]	7	–	–	1	I-PU/ O-OC	1	2 mA
VS2#/ B_GPSTB	**Voltage Sense 2 / General-Purpose Strobe B:** Connect to pin 57 on PC Card socket, or use as a general-purpose input port strobe to sense VS1 and VS2 through external hardware along with other external inputs.[a] [c]	144	–	–	1	I-PU/ O-OC	1	2 mA
GPSTB	**General-Purpose Strobe:** Connect A_GPSTB to pin 43 and B_GPSTB to pin 57 on PC Card socket, or use as a general-purpose input port strobe to sense VS1 and VS2 through external hardware along with other external inputs.[b] [c]	–	6	7	1	I-PU/ O-OC	1	2 mA

[a] VS1# and VS2# levels accessible by reading 'Socket B' (index 6Eh/6Fh) **External Data** register at extended index 0Ah.

[b] General-purpose strobe controlled by 'Socket A' (index 2Eh/2Fh) **Extension Control 2** register at extended index 0Bh.

[c] General-purpose strobe controlled by 'Socket B' (index 6Eh/6Fh) **Extension Control 2** register at extended index 0Bh.

Table 2-4. Power Control Pins

Pin Name	Description	Pin Number			Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/CL-PD6722					
			Socket A	Socket B				
VPP_VCC	This output is used to enable the socket V_{CC} supply onto the V_{PP} pin. This pin is mutually exclusive with VPP_PGM.	3	2	205	1	O	1	12 mA
VPP_PGM	This output is used to enable the programming voltage supply onto the V_{PP} pin. This pin is mutually exclusive with VPP_VCC.	2	1	204	1	O	1	12 mA
-VCC_3	This output is used to enable a 3.3V supply onto the V_{DD} socket. This pin is mutually exclusive with -VCC_5.	5	4	206	1	O	1	12 mA
-VCC_5	This output is used to enable a 5V supply onto the V_{DD} socket. This pin is mutually exclusive with -VCC_3.	6	5	207	1	O	1	12 mA

Table 2-5. Power and Ground Pins

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		CL-PD6712	CL-PD6720/ CL-PD6722				
+5V	This pin is connected to the system's 5-volt power supply. In systems where 5 volts is not available, this pin can be connected to the system's 3.3-volt supply (but 5-volt-only PC Cards will not be supported).	1	208	1	PWR	–	–
CORE_VDD	This pin provides power to the core circuitry of the CL-PD67XX. It can be connected to either a 3.3- or 5-volt power supply, independent of the operating voltage of other interfaces. For power conservation on a system with a 3.3-volt supply available, this pin should be connected to the 3.3-volt supply even if there is no intention of operating other interfaces on the device at less than 5 volts.	16, 91	27, 133	2	PWR	–	–
GND	All ground pins should be connected to system ground.	20, 54, 72, 78, 128, 133	31, 70, 79, 111, 140, 192	6	GND	–	–

Table 2-6 below summarizes the pin usage.

Table 2-6. Pin Usage Summary

Pin Group	Pin Quantity	
	CL-PD6712	CL-PD6720/ CL-PD6722
ISA bus interface pins	69	69
Socket interface pins	60	120
General-purpose strobe / voltage sense pins	2	2
Power control pins	4	8
Power and ground pins	9	9
Total:	144	208

2.4 Power-On Configuration Summary

On the rising edge of PWRGOOD, the CL-PD67XX latches the configuration pin SPKR_OUT*/C_SEL to determine which sockets are addressed by this device. A '1' on the SPKR_OUT*/C_SEL pin will cause the device to address Socket 0 (and Socket 1 for the CL-PD6720 and CL-PD6722). A '0' on this pin will cause the device to address Socket 2 (and Socket 3 for the CL-PD6720 and CL-PD6722).

Table 2-7. Chip Configuration at Power-up for Socket Support

SPKR_OUT*/C_SEL Level at Rising Edge of PWRGOOD	CL-PD6712	CL-PD6720 and CL-PD6722	
	Socket Interface Support	Socket A Interface Support	Socket B Interface Support
High	PC Card Socket 0 3E0 Index 00h–3Fh	PC Card Socket 0 3E0 Index 00h–3Fh	PC Card Socket 1 3E0 Index 40h–7Fh
Low	PC Card Socket 2 3E0 Index 80h–BFh	PC Card Socket 2 3E0 Index 80h–BFh	PC Card Socket 3 3E0 Index C0h–FFh

3. INTRODUCTION

3.1 System Architecture

This section describes PC Card basics, windowing, interrupts, CL-PD67XX power management, socket power management, write FIFO, bus sizing, programmable PC Card timing, and ATA and DMA mode operation.

3.1.1 PC Card Basics

PCMCIA is an abbreviation for Personal Computer Memory Card International Association. PC Card Standard[1] is a standard for using memory and I/O devices as insertable, exchangeable peripherals for PCs (personal computers) and handheld computers. For simpler end-user and vendor implementation of the standard, systems employing PC Card Standard should also be backward-compatible with industry-standard PC addressing.

The memory information for memory-type PC Cards must be mapped into the system memory address space. This is accomplished with a 'windowing' technique that is similar to expanded memory schemes already used in PC systems (for example, LIM 4.0 memory manager).

PC Cards can have *attribute* and *common* memory. Attribute memory is used to indicate to host software the capabilities of the PC Card, and it allows host software to change the configuration of the card. Common memory can be used by host software for any purpose (such as flash file system, system memory, and floppy emulation).

I/O-type PC Cards, such as modems, should also be directly addressable, as if the cards were I/O devices plugged into the ISA bus. For example, it would be highly desirable to have a PC Card modem accessible to standard communications software as if it were at a COM port. For COM1, this would require that the modem be accessed at system I/O address 3F8h–3FFh. The method of mapping a PC Card I/O address into anticipated areas of ISA I/O space is done similarly to memory windowing.

I/O-type PC Cards usually have interrupts that need to be serviced by host software. For the example of a modem card accessed as if at COM1, software would expect the modem to generate interrupts on the IRQ4 line. To be sure all interrupts are routed as expected, the CL-PD67XX can steer the interrupt from the PC Card to one of several standard PC interrupts (see Section 3.1.4 and the **Interrupt and General Control** register).

3.1.2 CL-PD67XX Windowing Capabilities

For full compatibility with existing software, and to ensure compatibility with future memory cards and software, the CL-PD67XX provides five programmable memory windows per socket and two programmable I/O windows per socket. These windows can be used by an inserted PC Card to access ISA memory and I/O space.

Having five memory windows per socket allows a memory-type card to be accessed through four memory windows programmed for common memory access (allowing PC-type expanded-memory-style management), leaving the fifth memory window available to be programmed to access the card's attribute memory without disrupting the common memory in use.

[1] The CL-PD67XX is backward-compatible with PCMCIA standards 1.0, 2.0, 2.01, and 2.1. The CL-PD67XX is also compatible with JEIDA 4.1 and its earlier standards corresponding with the PCMCIA standards above.

Each of the five memory windows has several programming options, including:

Memory Window Option	Description
Enabled	Each of the five memory windows can be individually enabled. Disabled windows are not responded to.
Start Address	The starting address of the window is programmable on 4-Kbyte boundaries starting at 64 Kbytes (1000h) with a maximum address of 16 Mbyte.
End Address	The ending address of the window is programmable on 4-Kbyte boundaries starting at 64 Kbytes (1000h) with a maximum address of 16 Mbyte. Only memory accesses between the starting and ending address are responded to.
Offset Address	The offset address is added to the ISA address to determine the address for accessing the PC Card. This allows the addresses in the PC Card address space to be different from the ISA address space.
Data Size	The size of accesses can be set manually to either 8 or 16 bits.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.
Register Access Setting	The -REG pin can be enabled on a per-window basis so that any of the windows can be used for accessing attribute memory.
Write Protect	If the window is programmed to be write-protected, then writes to the memory window are ignored (reads are still performed normally).

Each of the two I/O windows has several programming options, including:

I/O Window Option	Description
Enabled	Each of the two I/O windows can be individually enabled.
Start Address	The starting address of the window is programmable on single-byte boundaries from 0 to 64 Kbytes.
End Address	The ending address of the window is also programmable on single-byte boundaries from 0 to 64 Kbytes.
Offset Address	The offset address is added to the ISA address to determine the address for accessing the PC Card.
Auto Size	The size of accesses can be set automatically, based on the PC Card -IOIS16 signal.
Data Size	The size of accesses can be set manually to either 8 or 16 bits, overriding the Auto Size option.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.

CAUTION: The windows of the CL-PD67XX should never be allowed to overlap with each other or the other devices in the system. This would cause collisions in the IOCS16*, MEMCS16*, IOCHRDY, and SD[15:0] signals, resulting in erratic behavior.

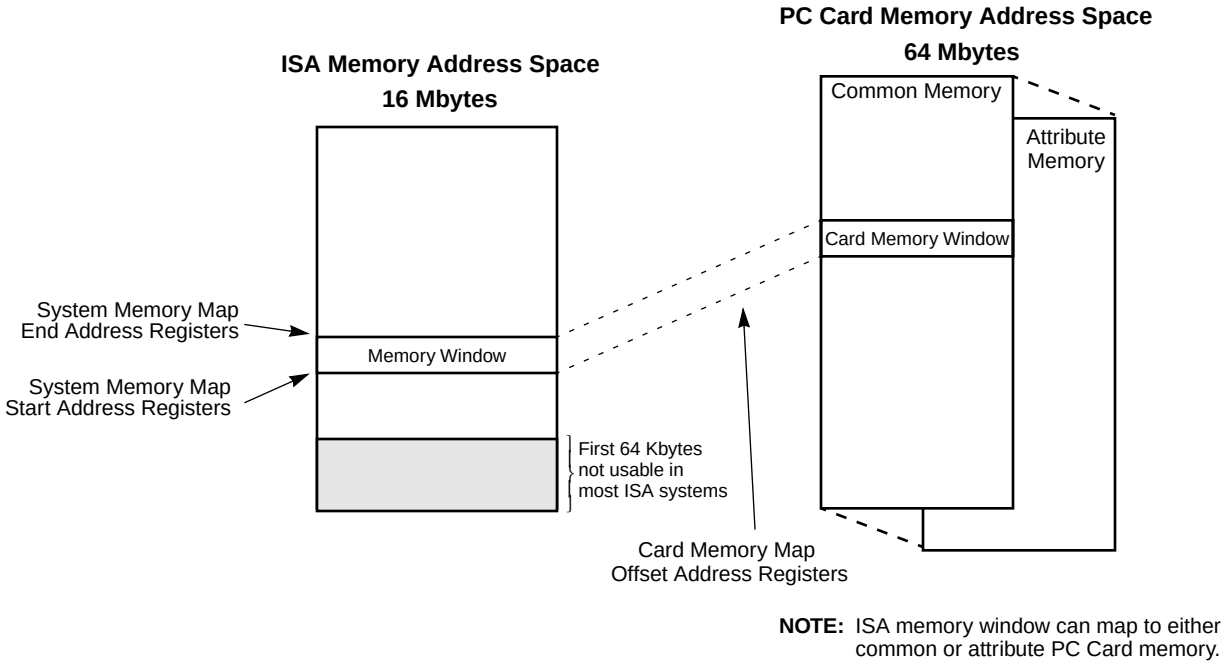


Figure 3-1. Memory Window Organization

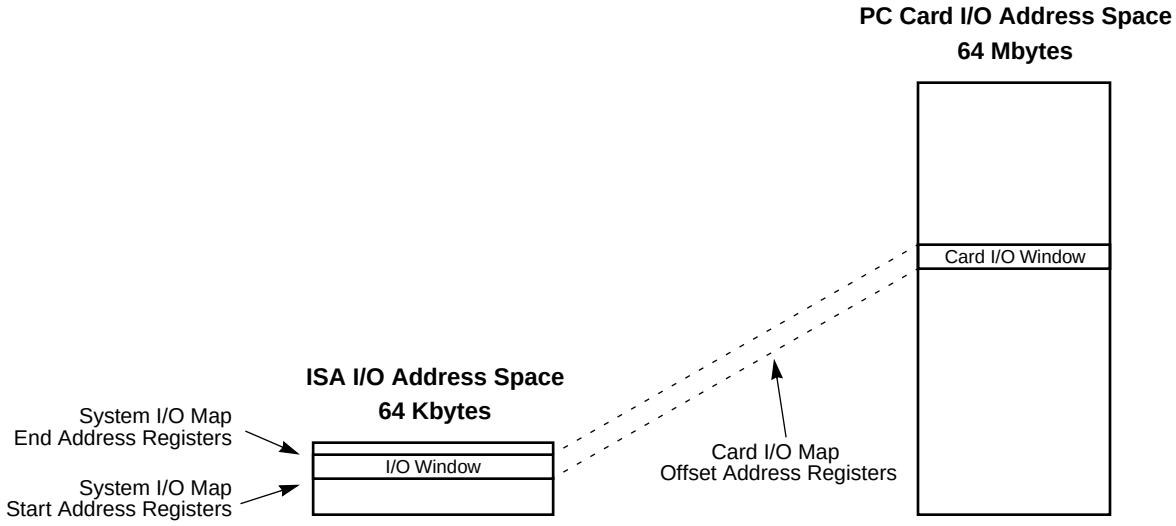


Figure 3-2. I/O Window Organization

3.1.3 CL-PD67XX Functional Blocks

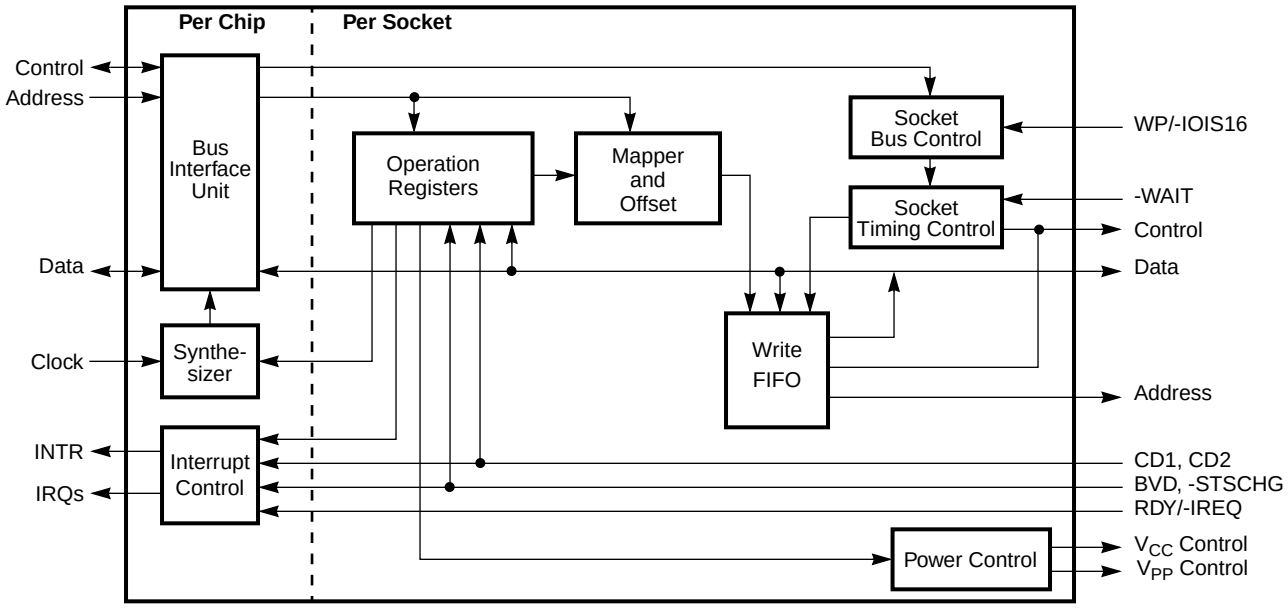


Figure 3-3. Functional Block Diagram

3.1.4 Interrupts

The CL-PD67XX provides ten interrupt pins that are labeled with names suggesting their mapping in the system, though there are no hard requirements specifying the exact mapping. Typically, all ten interrupt pins should be connected to system interrupt signals to allow maximum flexibility in programming interrupt routing from the CL-PD67XX.

Classes of Interrupts

The CL-PD67XX supports two classes of interrupts:

- Socket or card interrupts initiated by the PC Card activating its RDY/-IREQ signal
- Management interrupts triggered by changes in PC Card status, including:
  - — Card insertion or removal
  - — Battery warning indicator (BVD2) change on a memory-type card
  - — Battery dead indicator (BVD1) or I/O-type card status change (-STSCHG)
  - — Ready (RDY) status change on a memory-type card

Either class of interrupts can be routed to any of the ten interrupt pins on the CL-PD67XX.

Connection of Interrupt Pins

IRQ interrupts in PC-compatible systems are not generally shared by hardware. Therefore, each device in the system using IRQ interrupts must have a unique interrupt line. Additionally, many software applications assume that certain I/O devices use specific IRQ signals. To allow PC Cards with differing I/O functionalities to be connected to appropriate non-conflicting IRQ locations, the CL-PD67XX can steer the interrupt signal from a PC Card to any one of the ten different hardware interrupt lines.

For some I/O-type cards, software is written so that IRQ interrupts can be shared. The CL-PD67XX contains unique logic that allows IRQ interrupts to be shared under software control. This is accomplished by programming the CL-PD67XX to alternately pulse and then three-state the desired interrupt pin, which has been programmed as an IRQ output. This unique IRQ interrupt sharing technique can be controlled through software so that systems incapable of IRQ sharing have no loss of functionality.

3.1.5 Alternate Functions of Interrupt Pins

The CL-PD6720 has two interrupt pins that can be programmed for alternate functions: IRQ12/LED_OUT* and IRQ15/RI_OUT*. In addition, the CL-PD6712 and CL-PD6722 allow IRQ9 and IRQ10 to be programmed for system DMA transfer handshake functions.

3.1.5.1 IRQ12 as LED_OUT* Driver

If a disk-activity or card-cycle-activity indicator is desired, IRQ12/LED_OUT* can be programmed as an open-collector LED driver, capable of driving most common LEDs. There is no specific bit that programs the IRQ12 pin to become an LED driver; instead, whenever a socket interface is programmed to support a drive status LED input or is programmed to show card activity on the LED (as described below), the IRQ12 pin becomes reconfigured as an open-collector LED driver.

The **Extension Control 1** register's LED Activity Enable bit (extended index 03h bit 2) is used to enable the LED being used to show card activity. When this bit is set, any type of read or write cycles to the respective socket cause the IRQ12/LED_OUT* signal to be driven low for the duration of the card activity.

The Drive LED Enable bit (**Misc Control 2** register bit 4) is used to enable the BVD2/-SPKR/-LED input from an I/O-interfaced card to be interpreted as a drive LED input, where an open-collector signal driven low on this input will cause the IRQ12/LED_OUT* open-collector output to go low.

Any combination of settings of LED Activity Enable and Drive LED Enable bits can be used on each socket, with each type of activity being able to separately cause the LED to be illuminated. Status from non-present or non-activated cards is automatically masked off from causing the IRQ12/LED_OUT* signal to be driven low.

3.1.5.2 IRQ15 as RI_OUT*

If the capability to 'wake up' a system on an incoming phone call to a PC Card modem is desired, it may be necessary in some systems to use a dedicated wakeup signal to the system's SMI or NMI controller to facilitate this instead of using the normal interrupt connections. If this is the case, the IRQ15 connection can be reprogrammed to pass through a qualified version of an I/O interfaced card's -RI signal.

IRQ15/RI_OUT* is programmed as RI_OUT* by programming the IRQ15 Is RI Out bit (**Misc Control 2** register 1Eh bit 7) to '1'. Then if a particular socket supporting a modem is to have its BVD1/-STSCHG/-RI pin passed to the IRQ15/RI_OUT* pin, that socket's Ring Indicate Enable bit (**Interrupt and General Control** register 03h bit 7) should be set to '1'.

When the CL-PD67XX is configured this way, a low level at the BVD1/-STSCHG/-RI pin on an I/O interfaced PC Card will cause the IRQ15/RI_OUT* signal to become active-low (because it is intended to be connected to an SMI* or NMI* input on the system processor or core logic). To prevent multiple SMI or NMI interrupts from occurring on one ring condition, the IRQ15/RI_OUT* pin remains low until ISA bus activity resumes, indicated by the resumption of ISA bus memory or I/O reads or writes.

3.1.5.3 IRQ9 as DACK* and IRQ10 as DRQ

When a CL-PD6712 or CL-PD6722 is to be used for DMA support, IRQ9 is programmed as a DACK* input from an ISA bus DACK* signal selected by the system designer. Similarly, IRQ10 is programmed as an active-high DRQ output to the ISA bus and should be connected to the system bus DRQ signal corresponding to that used for DACK*.

IRQ9 and IRQ10 are thus redefined for DMA cycle support by the setting of the DMA System bit (**Misc Control 2** register 1Eh, bit 6) to '1'. Setting the DMA System bit redefines these ISA interface signals but does not cause DMA to a card to be enabled.

3.1.6 General-Purpose Strobe Feature

The CL-PD67XX has capability to use two pins as general-purpose strobes. This is a feature that causes a pin programmed as a general-purpose strobe to appear in software as an extended register in the CL-PD67XX register set, while in reality accesses to this extended register cause the general-purpose strobe pin to go active during the reg-

ister access. The strobe can be programmed to activate on reads or writes to this virtual extended register, allowing straightforward single-chip implementation of an 8-bit general purpose read or write port.

Chapter 12 provides detailed information on how this port can be used.

3.1.7 Voltage Sense Pins

The CL-PD6712 provides on-chip voltage sensing through the VS1#/A_GPSTB and VS2#/B_GPSTB pins. These can be directly connected to the VS1 and VS2 pins on a PC Card socket to allow card services and socket services software to sense card operating voltage ranges.

The CL-PD6720 and CL-PD6722 can also be simply configured for dual-socket VS1 and VS2 detection with an external read port consisting of half of a '244 buffer or other similar device, enabled by the B_GPSTB pin programmed as a read port.

The programming model for detecting VS1 and VS2 levels is identical for either implementation.

Chapter 13 provides detailed information on the programming model for VS1 and VS2 detection and how connections are made to achieve this functionality.

3.1.8 CL-PD67XX Power Management

To provide the longest possible battery life, the CL-PD67XX provides many power management features, including Low-Power Dynamic mode, Suspend mode, and control of PC Card socket power.

Low-Power Dynamic mode is transparent to the ISA bus. After reset, the CL-PD67XX is configured for Low-Power Dynamic mode. This mode can be turned off by setting **Misc Control 2** register, bit 1 to '0'. When in Low-Power Dynamic mode, periods of inactivity (no activity on the PC Card bus and system accesses to chip registers or inserted cards are no longer being performed) cause the CL-PD67XX to enter a low-power state where the clock is turned off to most of the chip and the PC Card address and data lines are set to a static value. V_{CC} and V_{PP} power to the card is left unchanged. When there is activity present on the PC Card bus, or the system accesses CL-PD67XX registers, or PC Cards are inserted or removed from the socket, the CL-PD67XX enters its active state, services the transaction, and then returns to its low-power state.

A Suspend mode can also be programmed. The CL-PD67XX Suspend mode is the chip's lowest software-controlled power mode. The CL-PD67XX is put into Suspend mode by setting the **Misc Control 2** register, bit 2 to '1'. In Suspend mode, all the internal clocks are turned off, and only read/write access to the **Index** register and write access to the **Misc Control 2** register is supported. All accesses to the PC Cards are ignored when in Suspend mode. V_{CC} and V_{PP} power to the card is left unchanged (the system power management software is responsible for turning off power to the socket and entering Suspend mode). Interrupts and ring indicate signals are passed through to the system bus when in Suspend mode. To exit Suspend mode, the **Misc Control 2** register bit 2 must be reset to '0'. It requires 50 ms for the CL-PD67XX to restart the internal clock synthesizer and become active again.

In addition to the software suspend, if the system hold's the AEN signal of the CL-PD67XX high, a hardware-assisted Super-Suspend mode occurs where ISA inputs to the chip are internally shut off. Internal in the CL-PD67XX, the ISA inputs are ignored and floating conditions on the ISA bus will not cause high current flow in the CL-PD67XX ISA input receivers. Since the ISA bus inputs to the core logic of the CL-PD67XX are also not toggling when AEN is set high, power consumption is further reduced. Interrupts and ring indicate signals are passed through to the system bus when in Super-Suspend mode

The CL-PD67XX power can be further managed by controlling socket power as outlined in Section 3.1.9. Socket power can be turned on and off through software or automatically when cards are inserted or removed. The CL-PD67XX provides six pins per socket for controlling external logic to switch V_{CC} and V_{PP} voltages on and off and for sensing a card's operating voltage range. Cards can be turned off when not in use.

Table 3-1. CL-PD67XX Power-Management Modes

Mode Name	PWRGOOD Level	AEN	Misc Control 2 Register		Functionality	Typical Power Consumption (CORE_VDD = 3.3 V, ISA_VCC, SOCKET_VCC, and +5V = 5.0 V)
			Suspend Mode (Bit 2)	Low-Power Dynamic Mode (Bit 1)		
Low-Power Dynamic (Default)	High	Normal	0	1	Full functionality	< 45 mW high activity, 9–14 mW normal system activity
Normal	High	Normal	0	0	Full functionality	< 85 mW high activity, 18 mW normal system activity
Suspend (Software Controlled)	High	Normal	1	–	8-bit access to **Misc Control 2** register. No other register access. No card in socket(s).	< 2 mW
Super-Suspend (Hardware Controlled)	High	Static High	1	–	No register access. No card in socket(s). System bus signals disabled (clock off).	<< 1 mW
Reset	Low[a]	–	–	–	No register access. No card in socket(s). System bus signals disabled.	9–14 mW

[a] IOR*, IOW*, MEMR*, and MEMW* must be held high when PWRGOOD is low to prevent manufacturing test mode outputs from driving the system data bus.

3.1.9 Socket Power Management Features

Card Removal

When a card is removed from a socket, the CL-PD67XX by default automatically disables the V_{CC} and V_{PP} supplies to the socket. If **Extension Control 1** register bit 1 is '0', card power is prevented from being automatically disabled when a card is removed. The CL-PD67XX can also be configured to have management interrupts notify software of card removal.

Card Insertion

Power to the socket is off at reset and whenever there is no card in a socket. When a card is detected (card detect input pins, -CD1 and -CD2, to the CL-PD67XX become asserted low), two independent actions can be programmed to occur.

If the CL-PD67XX has been set for automatic power-on (**Power Control** register bits 4 and 5 are both '1's), the CL-PD67XX automatically enables the socket V_{CC} supply (and, if so programmed, V_{PP} supply).

If the CL-PD67XX has been programmed to cause management interrupts for card-detection events, assertion of -CD1 and -CD2 to the CL-PD67XX causes a management interrupt to inform system software that a card was inserted. In the case of manual power detection (**Power Control** register bits 5 is '0'), system software can then determine the card's operating voltage range and then power-up the socket and initialize the card (or simply initialize the card if programmed for automatic power-on (**Power Control** register bits 5 is '1' and **Extension Control 1** register bit 1 is '1')).

3.1.10 Write FIFO

To increase performance when writing to PC Cards, two, independent, four-word-deep write FIFOs are used. Writes to PC Cards will complete without wait states until the FIFO is full. Register states should not be changed until the write FIFO is empty.

3.1.11 Bus Sizing

The CL-PD67XX incorporates logic to automatically detect its connection to 8- or 16-bit buses. This is accomplished by sensing SBHE* input activity. If the SBHE* pin is always high (that is, tied to ISA_VCC), the CL-PD67XX operates in 8-bit mode where all transfers occur on the lower data bus, bits 7:0. Any occurrence of the SBHE* going low triggers the CL-PD67XX to operate thereafter as a 16-bit device. 16-bit operation of the CL-PD67XX is properly triggered when the SBHE* input is connected to the system's SBHE* signal. When the CL-PD67XX is operating in 16-bit mode, all ISA bus transactions are 16-bit whenever possible, even if installed PC cards only support 8-bit transfers. In 16-bit mode, the signals SBHE* and SA0 are used to specify the width of the data transfer and the location of data on the bus (which byte lane has the data) during 8-bit transfers. The possible combinations for SBHE* and SA0 are shown in Table 3-2 and Table 3-3.

Table 3-2. 16-Bit Mode Operation

16-Bit Mode Transfer Types	SBHE*	SA0
Word	0	0
Upper Byte/Odd Address	0	1
Low Byte/Even Address	1	0
Not Valid	1	1

Table 3-3. 8-Bit Mode Operation

8-Bit Mode Transfer Types[a]	SA0
Even Address	0
Odd Address	1

[a] The SBHE* signal is pulled up. If the SBHE* signal remains high, the CL-PD67XX causes all transfers to occur on D[7:0] only.

Typically, there are three types of data transfers to and from the CL-PD67XX:

- **16-Bit Transfer from 16-Bit Processor —** The CPU puts the address on the bus. Then the CL-PD67XX identifies the address on the bus as either an 8- or 16-bit transfer. If the transfer is identified as 16-bit, the host acknowledges with the appropriate signal, either MEMCS16* or IOCS16*. Data is transferred to/from the data bus as a word on both byte lanes.
- **8-Bit Transfer from 16-Bit Processor —** The CPU puts the address on the bus. Then the CL-PD67XX identifies the address on the bus as either an 8- or 16-bit transfer. In this case, the transfer is identified as an 8-bit transfer. The host queries SA0 and SBHE* to determine the byte lane on which the transfer is to occur. The data is transferred to/from the data bus (see Table 3-2).
- **8-Bit Transfer from 8-Bit Processor —** The CPU puts the address on the bus. The host determines that it will be an 8-bit transfer since the SBHE* signal has been tied high. The CL-PD67XX queries SA0 to determine if the byte is odd/even. The data is transferred to/from the Data bus (D[7:0]).

3.1.12 Programmable PC Card Timing

The Setup, Command, and Recovery time for the PC Card bus is programmable (see Chapter 10). The CL-PD67XX can be programmed to match the timing requirements of any PC Card. There are two sets of timing registers, Timer Set 0 and Timer Set 1, that can be selected on a per-window basis for both I/O and memory windows.

To be compatible with the 82365SL, the two timing sets are programmed at the rising edge of PWRGOOD to include normal-wait and one-wait-state timing.

3.1.13 ATA Mode Operation

The CL-PD67XX supports direct connection to AT-attached-interface hard drives. ATA drives use an interface very similar to the IDE interface found on many popular portable computers. In this mode, the address and data conflict with the floppy drive is handled automatically. See Chapter 11 for more information.

3.1.14 DMA Mode Operation for the CL-PD6712 and CL-PD6722

A slave mode Direct Memory Access (DMA) feature exists in the CL-PD6712 and CL-PD6722. To use DMA mode, the **Interrupt and General Control** register, bit 5 must be set to '1' to operate the PC Card in I/O Card Interface mode. PC Card interface DMA handshake signal options must also be selected. Refer to the description of the **Extension Control 1** register on page 66 as well as Chapter 14.

3.1.15 Selective Data Drive for I/O Windows

The CL-PD67XX can be programmed to drive only some of the ISA bus data pins on reads from I/O windows. This reduces data contention for I/O addresses that include more than one peripheral. In the standard IBM® PC AT, I/O map, floppy disk, and hard disk share address 3F7h. The floppy disk drives ISA-data-bus bit 7 on a read from 3F7h, and the hard disk drives bits 6:0. To allow both floppy disk controllers on the motherboard and hard disks on the PC Card bus (or vice versa) to coexist, the CL-PD67XX can be programmed through use of its Data Mask registers to disable bit 7 on I/O reads at addresses 3F7h and 377h. This is done by programming up I/O windows to these addresses as part of the task of configuring a socket for ATA drive support (see page 65). Alternately, all bits except bit 7 can also be disabled to allow the opposite case.

3.2 Host Access to Registers

The CL-PD67XX registers are accessed through an 8-bit indexing mechanism. An index register scheme allows a large number of internal registers to be accessed by the CPU using only two I/O addresses.

The **Index** register (see Chapter 5) is used to specify which of the internal registers the CPU will access next. The value in the **Index** register is called the Register Index. This number specifies a unique internal register. The **Data** register is used by the CPU to read and write the internal register specified by the **Index** register.

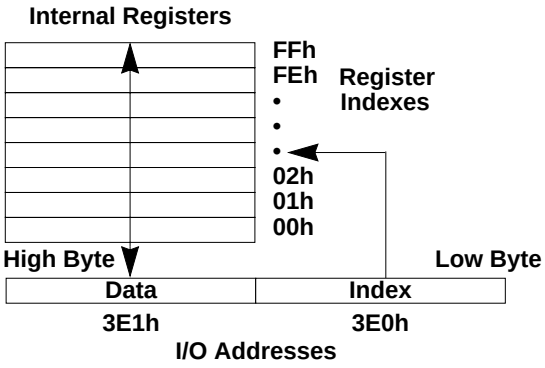


Figure 3-4. Indexed 8-Bit Register Structure

The following code segment demonstrates use of an indexed 8-bit register:

```
mov dx, 3E0h
mov al, 02h
mov ah, 3Ch
out dx, ax
```

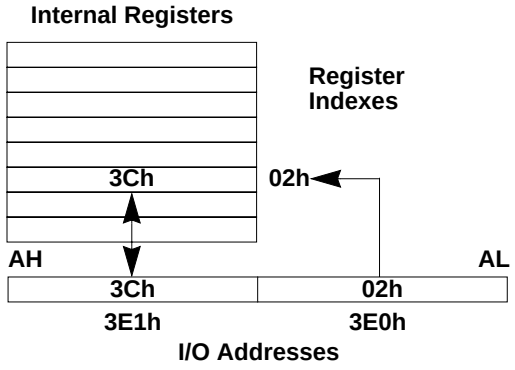


Figure 3-5. Indexed 8-Bit Register Example

Double-Indexed Registers

The CL-PD67XX has Extension registers that add to the functionality of the 82365SL-compatible register set. Within the Extension registers is an **Extended Index** register and **Extended Data** register that provide access to more registers. The registers accessed through **Extended Index** and **Extended Data** are thus double indexed. The example below shows how to access the **Extension Control 1** register, one of the double-indexed registers.

```
;Write to Extension Control 1 register example

;Constants section
   Extended_Index      EQU 2Eh
   Index_Reg           EQU 2Fh
   Ext_Cntrl_1         EQU 03h
   PD67XX_Index        EQU 3E0h

;Code section
   mov   dx, PD67XX_Index
   mov   al, Extended_Index
   mov   ah, Ext_Cntrl_1
   out   dx, ax
   mov   al, Index_Reg
   mov   ah, user_data         ;Desired data to be
   out   dx, ax                ;written to
                               ;extended index 03h

;Read from Extension Control 1 register example

;Code section
   mov   dx, PD67XX_Index
   mov   al, Extended_Index
   mov   ah, Ext_Cntrl_1
   out   dx, ax
   mov   al, Index_Reg
   out   dx, al
   inc   dx                    ;al has extended
   in    al, dx                ;index 03h data
```

3.3 Power-On Setup

Following reset, the CL-PD67XX must be configured by host software. The host software's setup procedure is different depending on its PC system configuration, in particular, the power supply arrangement.

The application of the RESET signal (see page 18) on power-up causes initialization of all the CL-PD67XX register bits and fields to their reset values. Not all registers have reset values; only registers with bits and fields specified to have reset values are initialized.

One bit, which is loaded on hardware reset from the SPKR_OUT*/C_SEL pin (see page 15), is used to determine which socket the CL-PD67XX will respond to.

4. REGISTER DESCRIPTION CONVENTIONS

Register Headings

The description of each register starts with a header containing the following information:

Header Field	Description
Register Name	Indicates the register name.
Index [a]	The Index value through which an internal register in an indexed register set is accessed.
Register Per	Indicates whether the register affects both sockets, marked *chip*, or an individual socket, marked *socket*. If *socket* is indicated, there are two registers being described, each with a separate Index value (one for each socket, A and B). [a]
Register Compatibility Type	Indicates whether the register is 82365SL-compatible, marked *365* or a register extension, marked *ext*.

[a] When the register is socket-specific, the Index value given in the register heading is for Socket A only. For the Socket B register on the CL-PD6720 and CL-PD6722, add 40h to the Index value of the Socket A register.

Special Function Bits

Following is a description of bits with special functions:

Bit Type	Description
Reserved	These bits are Reserved and should not be changed.
Compatibility Bit	These bits have no function on the CL-PD67XX, but are included for compatibility with the 82365SL register set.
0 or *1*	These read-only bits are forced to either '0' or '1' at reset and cannot be changed.
Scratchpad Bit	These read/write bits are available for use as bits of memory.

Bit Naming Conventions

The following keywords are used within bit and field names:

Keyword	Description
Enable	Indicates that the function described in the rest of the bit name is active when the bit is '1'.
Disable	Indicates that the function described in the rest of the bit name is active when the bit is '0'.
Mode	Indicates that the function of the bit alters the interpretation of the values in other registers.
Input	Indicates a bit or field that is read from a pin.
Output	Indicates a bit or field that is driven to a pin.
Select	Indicates that the bit or field selects between multiple alternatives. Fields that contain *Select* in their names have an indirect mapping between the value of the field and the effect.
Status	Indicates one of two types of bits: either Read-only bits used by the CL-PD67XX to report information to the system or bits set by the CL-PD67XX in response to an event, and can also be cleared by the system. The system cannot directly cause a Status bit to become '1'.
Value	Indicates that the bit or field value is used as a number.

Read/Write Convention

Bit Access	Description
RW:n	Bit is read/write and resets to value *n* when PWRGOOD is cycled.
R	Bit is read-only and setting is determoned by conditions noted. Set this bit to '0', or echo back value read.
R:n	Bit is read-only and resets to value *n* when PWRGOOD is cycled. Set this bit to '0', or echo back value read.
R:n W:m	Bit is read/write and resets to value *n* when PWRGOOD is cycled. Set this bit to value *m* only.

5. OPERATION REGISTERS

The CL-PD67XX's internal registers are accessed through a pair of Operation registers — an **Index** register and a **Data** register. The **Index** register is accessed at address 03E0h, and the **Data** register is accessed at 03E1h.

5.1 Index

Register Name: **Index** *Index:* **n/a**							*Register Per:* chip *Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Device Index	Socket Index	Register Index					
RW:0	RW:0	RW:000000					

The **Data** register is accessed at at 03E1h.

Bits 5:0 — Register Index

These bits determine which of the 64 possible socket-specific registers will be accessed when the **Data** register is next accessed by the processor. Note that some values of the Register Index field are reserved, see Table 5-1.

Bit 6 — Socket Index

This bit determines which set of socket-specific registers is currently selected. When this bit is '0', a Socket A register is selected. When this bit is '1', a Socket B register is selected. Note that the CL-PD6712 supports one socket, and the CL-PD672X supports two sockets.

Bit 7 — Device Index

In systems where two CL-PD67XXs are used, this bit differentiates between them.

The **Index** register value determines which internal register should be accessed (read or written) in response to each CPU access of the **Data** register. Each of the possible PC Card sockets is allocated 64 of the 256 locations in the internal register index space.

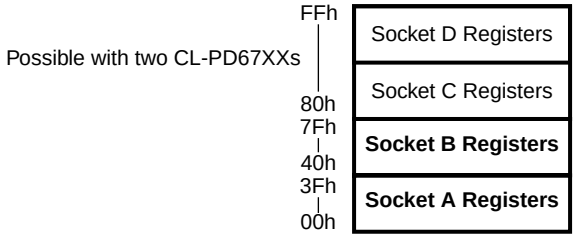


Figure 5-1. Device/Socket/Register Index Space

When viewed as a 8-bit value, the contents of the **Index** register completely specify a single internal-register byte. For example, when the value of this register is in the range 00h–3Fh, a Socket A register is selected (Socket Index bit is '0'), and when the value of this register is in the range 40h–7Fh, a Socket B register is selected (Socket Index bit is '1'). This register only reads back for Device 0. Device 1 will read back only the upper data byte when 16-bit reads occur at 3E0h.

The internal register that is accessed when the CPU reads or writes the **Data** register is determined by the current value of the **Index** register, as follows:

Table 5-1. Index Registers

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B[a]		
Chip Revision	00h[b]		Chapter 6: Chip Control	37
Interface Status	01h	41h		38
Power Control	02h	42h		40
Interrupt and General Control	03h	43h		42
Card Status Change	04h	44h		44
Management Interrupt Configuration	05h	45h		45
Mapping Enable	06h	46h		47
I/O Window Control	07h	47h	Chapter 7: I/O Window Mapping	49
System I/O Map 0 Start Address Low	08h	48h		50
System I/O Map 0 Start Address High	09h	49h		50
System I/O Map 0 End Address Low	0Ah	4Ah		51
System I/O Map 0 End Address High	0Bh	4Bh		51
System I/O Map 1 Start Address Low	0Ch	4Ch		50
System I/O Map 1 Start Address High	0Dh	4Dh		50
System I/O Map 1 End Address Low	0Eh	4Eh		51
System I/O Map 1 End Address High	0Fh	4Fh		51
System Memory Map 0 Start Address Low	10h	50h	Chapter 8: Memory Window Mapping	53
System Memory Map 0 Start Address High	11h	51h		54
System Memory Map 0 End Address Low	12h	52h		54
System Memory Map 0 End Address High	13h	53h		55
Card Memory Map 0 Offset Address Low	14h	54h		56
Card Memory Map 0 Offset Address High	15h	55h		56
Misc Control 1	16h	56h	Chapter 9: Extension	58
FIFO Control	17h	57h		60
System Memory Map 1 Start Address Low	18h	58h	Chapter 8: Memory Window Mapping	53
System Memory Map 1 Start Address High	19h	59h		54
System Memory Map 1 End Address Low	1Ah	5Ah		54
System Memory Map 1 End Address High	1Bh	5Bh	Chapter 8: Memory Window Mapping	55
Card Memory Map 1 Offset Address Low	1Ch	5Ch		56
Card Memory Map 1 Offset Address High	1Dh	5Dh		56
Misc Control 2	1Eh[b]		Chapter 9: Extension	61
Chip Information	1Fh[b]			63
System Memory Map 2 Start Address Low	20h	60h	Chapter 8: Memory Window Mapping	53
System Memory Map 2 Start Address High	21h	61h		54
System Memory Map 2 End Address Low	22h	62h		54
System Memory Map 2 End Address High	23h	63h		55
Card Memory Map 2 Offset Address Low	24h	64h		56
Card Memory Map 2 Offset Address High	25h	65h		56

Table 5-1. Index Registers *(cont.)*

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B[a]		
ATA Control	26h	66h	Chapter 9: Extension	64
Scratchpad	27h	67h	–	–
System Memory Map 3 Start Address Low	28h	68h	Chapter 8: Memory Window Mapping	50
System Memory Map 3 Start Address High	29h	69h		54
System Memory Map 3 End Address Low	2Ah	6Ah		54
System Memory Map 3 End Address High	2Bh	6Bh		55
Card Memory Map 3 Offset Address Low	2Ch	6Ch		56
Card Memory Map 3 Offset Address High	2Dh	6Dh		56
Extended Index:	2Eh	6Eh	Chapter 9: Extension	65
Scratchpad	Extended index 00h			–
Data Mask 0	Extended index 01h			65
Data Mask 1	Extended index 02h			65
Extension Control 1 (formerly DMA Control)	Extended index 03h			65
Maximum DMA Acknowledge Delay	Extended index 04h			65
Reserved	Extended index 05h–09h			–
External Data	Extended index 0Ah			69
Extension Control 2	Extended index 0Bh			71
Extended Data	2Fh	6Fh		65
System Memory Map 4 Start Address Low	30h	70h	Chapter 8: Memory Window Mapping	50
System Memory Map 4 Start Address High	31h	71h		54
System Memory Map 4 End Address Low	32h	72h		54
System Memory Map 4 End Address High	33h	73h		55
Card Memory Map 4 Offset Address Low	34h	74h		56
Card Memory Map 4 Offset Address High	35h	75h		56
Card I/O Map 0 OffsetAddress Low	36h	76h	Chapter 7: I/O Window Mapping	52
Card I/O Map 0 Offset Address High	37h	77h		52
Card I/O Map 1 Offset Address Low	38h	78h		52
Card I/O Map 1 Offset Address High	39h	79h		52
Setup Timing 0	3Ah	7Ah	Chapter 10: Timing	72
Command Timing 0	3Bh	7Bh		73
Recovery Timing 0	3Ch	7Ch		74
Setup Timing 1	3Dh	7Dh		72
Command Timing 1	3Eh	7Eh		73
Recovery Timing 1	3Fh	7Fh		74

[a] Socket B is available on the dual-socket CL-PD6720 and CL-PD6722.

[b] This register affects both sockets (it is not specific to either socket).

5.2 Data

Register Name: **Data**							*Register Per:* chip
Index: **n/a**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Data							

The **Data** register is accessed at at 03E1h. This register indicates the contents of the register at the Device/Socket/Register Index selected by the **Index** register.

6. CHIP CONTROL REGISTERS

6.1 Chip Revision

Register Name: **Chip Revision** *Register Per:* chip
Index: **00h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Interface ID		*0*	*0*	Revision			
R:10		R:0	R:0	R:0010[a]			

[a] Value for the current stepping only.

Bits 3:0 — Revision

This field indicates compatibility with the 82365SL A-step.

Bits 7:6 — Interface ID

00	I/O only.
01	Memory only.
10	Memory and I/O.
11	Reserved.

These bits identify what type of interface this controller supports.

6.2 Interface Status

Register Name: **Interface Status** *Index:* **01h**							*Register Per:* socket *Register Compatibility Type:* 365
Bit 7 *-VPP_VALID*	*Bit 6*	*Bit 5* *RDY*	*Bit 4* *WP*	*Bit 3* *-CD2*	*Bit 2* *-CD1*	*Bit 1* *BVD2*	*Bit 0* *BVD1*
V_{PP} Valid	Card Power On	Ready/Busy*	Write Protect	Card Detect		Battery Voltage Detect	
R[a]	R:0	R[b]	R[c]	R[d]		R[e]	

[a] Bit 7 is the inversion of the value of the -VPP_VALID pin (see page 15).

[b] Bit 5 is the value of the RDY/-IREQ pin (see page 17).

[c] Bit 4 is the value of the WP/-IOIS16 pin (see page 17).

[d] Bits 3:2 are the inversion of the values of the -CD1 and -CD2 pins (see page 18).

[e] Bits 1:0 are the values of the BVD1/-STSCHG and BVD2/-SPKR pins (see page 18).

Bits 1:0 — Battery Voltage Detect

BVD2 Input Level	BVD1 Input Level	Bit 1	Bit 0	PC Card Interpretation
Low	Low	0	0	Card data lost
Low	High	0	1	Battery low warning
High	Low	1	0	Card data lost
High	High	1	1	Battery/data okay

These bits are used by PC Card support software and firmware to indicate the amount of capacity left in the battery in battery-backed cards in Memory Card Interface mode only. In I/O Card Interface mode, bit 0 indicates the state of the BVD1/-STSCHG pin (see page 18). Bit 1 status should be ignored in I/O Card Interface mode.

Bits 3:2 — Card Detect

-CD2 Level	-CD1 Level	Bit 3	Bit 2	Card Detect Status
High	High	0	0	Either no card or card is not fully inserted
High	Low	0	1	Card is not fully inserted
Low	High	1	0	Card is not fully inserted
Low	Low	1	1	Card is fully inserted

These bits indicate the state of the -CD1 and -CD2 pins (see page 18).

Bit 4 — Write Protect

0	Card is not write protected.
1	Card is write protected.

This bit indicates the state of the WP/-IOIS16 pin (see page 17) on the card and has meaning only in Memory Card Interface mode.

Bit 5 — Ready/Busy*

0	Card is not ready.
1	Card is ready.

This bit indicates the state of the RDY/-IREQ pin (see page 17) on the card. If the card has been configured for I/O, then this bit will not be valid.

Bit 6 — Card Power On

0	Power to the card is not on.
1	Power to the card is on.

This status bit indicates whether power to the card is on. Refer to the Table 5–1 for details.

Bit 7 — V_{PP} Valid

0	This status bit indicates a logic high at the -VPP_VALID pin.
1	This status bit indicates a logic low at the -VPP_VALID pin.

This bit indicates the status of the -VPP_VALID pin (see page 15).

6.3 Power Control

Register Name: **Power Control** *Index:* **02h**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Card Enable	*Compatibility Bit*	Auto-Power	V_{CC} Power	*Compatibility Bits*		$V_{PP}1$ Power	
RW:0	RW:0	RW:0	RW:0	RW:00		RW:00	

Table 6-1. Enabling of Socket Power Controls

PWR-GOOD Level	Power Control Register		-CD1 and -CD2 Both Active Low	Interface Status Register (see page 38)	-VCC_3 and -VCC_5 Levels	VPP1_PGM and VPP1_VCC Levels
	Bit 4: V_{CC} Power	Bit 5: Auto-Power		Bit 6: Card Power On		
Low	X	X	X	0	Inactive high	Inactive low
High	0	X	X	0	Inactive high	Inactive low
High	1	0	X	1	Activated per **Misc Control 1** register, bit 1	Activated per **Power Control** register, bits 1 and 0
High	1	1	No	0	Inactive high	Inactive low
High	1	1	Yes	1	Activated per **Misc Control 1** register, bit 1	Activated per **Power Control** register, bits 1 and 0

Table 6-2. Enabling of Outputs to Card Socket

PWR-GOOD Level	-CD1 and -CD2 Both Active Low	Power Control Register		CL-PD67XX Signal Outputs to Socket
		Bit 4: V_{CC} Power	Bit 7: Card Enable	
Low	X	X	X	High impedance
High	No	X	X	High impedance
High	Yes	0	0	High impedance
High	Yes	0	1	Enabled
High	Yes	1	0	High impedance
High	Yes	1	1	Enabled

Bit Name	Value	Description
V_{CC} Power	1	Enables V_{CC} to level described by V_{CC} 3.3V (see page 58)
Auto-Power	1	Enables Auto-power mode
Card Enable	1	Enables socket output drivers

Bits 1:0 — $V_{PP}1$ Power

$V_{PP}1$ Power Bit 1	$V_{PP}1$ Power Bit 0	VPP_PGM	VPP_VCC	PC Card Intended Socket Function
0	0	Inactive low	Inactive low	Zero volts to PC Card socket $V_{PP}1$ pin
0	1	Inactive low	Active high [a]	Selected card V_{CC} to PC Card socket $V_{PP}1$ pin
1	0	Active high [a]	Inactive low	+12V to PC Card socket $V_{PP}1$ pin
1	1	Inactive low	Inactive low	Zero volts to PC Card socket $V_{PP}1$ pin

[a] Under conditions where $V_{PP}1$ power is activated. See Table 6.3.

These bits are intended to be used to control the power to the $V_{PP}1$ pin of the PC Card.

Bit 4 — V_{CC} Power

0	Power is not applied to the card: the -VCC_3 and -VCC_5 socket power control pins are inactive high.
1	Power is applied to the card: if bit 5 is '0', or bit 5 is '1' and -CD2 and -CD1 are active low, then the selected -VCC_3 or -VCC_5 socket power control pin is active low.

Depending on the value of bit 5 below, setting this bit to '1' will cause power to be applied to the card. The V_{CC} 3.3V bit (see page 58) determines whether 3.3V or 5V power is applied.

Bit 5 — Auto-Power

0	V_{CC} and $V_{PP}1$ power control signals are activated independent of the socket's -CD2 and -CD1 input levels.
1	V_{CC} and $V_{PP}1$ power control signals are only activated if the socket's -CD2 and -CD1 inputs are active low.

When this bit is set to '1', the CL-PD67XX causes power to the card to be turned on and off automatically with the insertion and removal of a PC card from the socket.

Bit 7 — Card Enable

0	Outputs to card socket are not enabled and are floating.
1	Outputs to card socket are enabled if -CD1 and -CD2 are active low and bit 4 is '1'.

When this bit is '1', the outputs to the PC Card are enabled if a card is present and card power is being supplied. The pins affected include: -CE2, -CE1, -IORD, -IOWR, -OE, -REG, RESET, A[25:0], D[15:0], and -WE (see page 16).

6.4 Interrupt and General Control

Register Name: **Interrupt and General Control** *Index:* **03h**							*Register Per:* socket *Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Ring Indicate Enable	Card Reset*	Card Is I/O	Enable Manage Int	Card IRQ Select			
RW:0	RW:0	RW:0	RW:0	RW:0000			

Bits 3:0 — Card IRQ Select

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ 3
0100	IRQ 4
0101	IRQ 5
0110	Reserved
0111	IRQ 7
1000	Reserved
1001	IRQ 9 (On the CL-PD67X2, this output may alternately be used as an ISA bus DACK* signal)
1010	IRQ 10 (On the CL-PD67X2, this output may alternately be used as an ISA bus DRQ signal)
1011	IRQ 11
1100	IRQ 12 (This output may alternately be used for LED)
1101	Reserved
1110	IRQ 14
1111	IRQ 15 (This output may alternately be used for ring indicate)

These bits determine which IRQ will occur when the card causes an interrupt through the RDY/-IREQ pin on the PC Card connector.

Bit 4 — Enable Manage Int

0	Card status management interrupts occur as programmed by Management IRQ Select bits (bits 7:4 of **Management Interrupt Configuration** register, see page 46).
1	Card status management interrupts are redirected to the -INTR line instead of the programmed IRQ pin.

This bit determines how management interrupts will occur.

Bit 5 — Card Is I/O

0	Memory Card Interface mode: card socket configured to support memory cards. Dual-function socket interface pins perform memory card-type interface functions.
1	I/O Card Interface mode: card socket configured to support I/O/memory card-type interface functions. Dual-function socket interface pins perform I/O/memory card-type interface functions.

This bit determines how dual-function socket interface pins will be used.

Bit 6 — Card Reset*

0	The RESET signal to the card socket is set active (high for normal, low for ATA mode).
1	The RESET signal to the card socket is set inactive (low for normal, high for ATA mode).

This bit determines whether the RESET signal (see page 18) to the card is active or inactive. When the Card Enable bit (see page 41) is '0', the RESET signal to the card will be high-impedance. See Chapter 10 for further description of ATA mode functions.

Bit 7 — Ring Indicate Enable

0	BVD1/-STSCHG pin is status change function.
1	BVD1/-STSCHG pin is ring indicate input pin from card.

This bit determines whether the -STSCHG input pin is used to activate the IRQ15 pin in conjunction with **Misc Control 2**, IRQ15 Is RI Out (see page 62). This bit has no significance when the card socket is configured for memory card operation.

6.5 Card Status Change

Register Name: **Card Status Change** *Index:* **04h**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
0	*0*	*0*	*0*	Card Detect Change	Ready Change	Battery Warning Change	Battery Dead Or Status Change
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

This register indicates the source of a management interrupt generated by the CL-PD67XX.

NOTE: The corresponding bit in the **Management Interrupt Configuration** register must be set to '1' to enable each specific status change detection.

Bit 0 — Battery Dead Or Status Change

0	A transition (from high to low for memory card support or either high to low or low to high for I/O card support) on the BVD1/-STSCHG pin has not occurred since this register was last read.
1	A transition on the BVD1/-STSCHG pin has occurred.

When the socket is configured for memory card support, this bit is set to '1' when a BVD1 battery dead high-to-low transition has been detected. When the socket is configured for I/O card support, this bit is set to '1' when the BVD1/-STSCHG pin (see page 18) changes from either high to low or low to high. This bit is reset to '0' whenever this register is read. In I/O Card Interface mode, function of this bit is not affected by bit 7 of the **Interrupt and General Control** register.

Bit 1 — Battery Warning Change

0	A transition (from high to low) on the BVD2 pin has not occurred since this register was last read.
1	A transition on the BVD2 pin has occurred.

When a socket is configured for memory card support, this bit is set to '1' when a high-to-low transition on BVD2 occurs indicating a battery warning was detected. This bit should be ignored when the socket is configured for I/O card support. This bit is reset to '0' whenever this register is read.

Bit 2 — Ready Change

0	A transition on the RDY/-IREQ pin has not occurred since this register was last read.
1	A transition on the RDY/-IREQ pin has occurred.

When this bit is '1', a change has occurred in the card RDY/-IREQ pin (see page 17). This bit will always read 0 when the card is configured as an I/O card. This bit is reset to '0' whenever this register is read.

Bit 3 — Card Detect Change

0	A transition on the -CD1 or -CD2 pins has not occurred since this register was last read.
1	A transition on the -CD1 or -CD2 pins has occurred.

When this bit is '1', a change has occurred on the -CD1 or -CD2 pins (see page 18). This bit is reset to '0' whenever this register is read.

6.6 Management Interrupt Configuration

Register Name: **Management Interrupt Configuration** *Register Per:* socket
Index: **05h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Management IRQ Select				Card Detect Enable	Ready Enable	Battery Warning Enable	Battery Dead Or Status Change Enable
RW:0000				RW:0	RW:0	RW:0	RW:0

This register controls which status changes may cause management interrupts and at which pin the management interrupts will appear.

Bit 0 — Battery Dead Or Status Change Enable

0	Battery Dead Or Status Change management interrupt disabled.
1	If Battery Dead Or Status Change is '1', a management interrupt will occur.

When this bit is '1', a management interrupt will occur when the **Card Status Change** register's Battery Dead Or Status Change bit (see page 44) is '1'. This allows management interrupts to be generated on changes in level of the BVD1/-STSCHG pin.

Bit 1 — Battery Warning Enable

0	Battery Warning Change management interrupt disabled.
1	If Battery Warning Change is '1', a management interrupt will occur.

When this bit is '1', a management interrupt will occur when the **Card Status Change** register's Battery Warning Change bit (see page 44) is '1'. This bit is ignored when the card socket is in I/O mode.

Bit 2 — Ready Enable

0	Ready Change management interrupt disabled.
1	If Ready Change is '1', a management interrupt will occur.

When this bit is '1', a management interrupt will occur when the **Card Status Change** register's Ready Change bit (see page 44) is '1'.

Bit 3 — Card Detect Enable

0	Card Detect Change management interrupt disabled.
1	If Card Detect Change is '1', a management interrupt will occur.

When this bit is '1', a management interrupt will occur when the **Card Status Change** register's Card Detect Change bit (see page 44) is '1'.

Bits 7:4 — Management IRQ Select

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ 3
0100	IRQ 4
0101	IRQ 5
0110	Reserved
0111	IRQ 7
1000	Reserved
1001	IRQ 9 (On the CL-PD67X2, this output may alternately be used as an ISA bus DACK* signal)
1010	IRQ 10 (On the CL-PD67X2, this output may alternately be used as an ISA bus DRQ signal)
1011	IRQ 11
1100	IRQ 12 (This output may alternately be used for LED)
1101	Reserved
1110	IRQ 14
1111	IRQ 15 (This output may alternately be used for ring indicate)

These bits determine which interrupt pin will be used for card status change management interrupts.

6.7 Mapping Enable

Register Name: **Mapping Enable** *Index:* **06h**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
I/O Map 1 Enable	I/O Map 0 Enable	MEMCS16 Full Decode	Memory Map 4 Enable	Memory Map 3 Enable	Memory Map 2 Enable	Memory Map 1 Enable	Memory Map 0 Enable
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0 — Memory Map 0 Enable

0	Memory Mapping registers for Memory Space 0 disabled.
1	Memory Mapping registers for Memory Space 0 enabled.

When this bit is '1', the Memory Mapping registers for Memory Space 0 will be enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 1 — Memory Map 1 Enable

0	Memory Mapping registers for Memory Space 1 disabled.
1	Memory Mapping registers for Memory Space 1 enabled.

When this bit is '1', the Memory Mapping registers for Memory Space 1 will be enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 2 — Memory Map 2 Enable

0	Memory Mapping registers for Memory Space 2 disabled.
1	Memory Mapping registers for Memory Space 2 enabled.

When this bit is '1', the Memory Mapping registers for Memory Space 2 will be enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 3 — Memory Map 3 Enable

0	Memory Mapping registers for Memory Space 3 disabled.
1	Memory Mapping registers for Memory Space 3 enabled.

When this bit is '1', the Memory Mapping registers for Memory Space 3 will be enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 4 — Memory Map 4 Enable

0	Memory Mapping registers for Memory Space 4 disabled.
1	Memory Mapping registers for Memory Space 4 enabled.

When this bit is '1', the Memory Mapping registers for Memory Space 4 will be enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 5 — MEMCS16 Full Decode

This bit is not used. All addresses are used to determine the level of MEMCS16*.

Bit 6 — I/O Map 0 Enable

0	I/O Mapping registers for I/O Space 0 disabled.
1	I/O Mapping registers for I/O Space 0 enabled.

When this bit is '1', the I/O Mapping registers for I/O Space 0 will be enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

Bit 7 — I/O Map 1 Enable

0	I/O Mapping registers for I/O Space 1 disabled.
1	I/O Mapping registers for I/O Space 1 enabled.

When this bit is '1', the I/O Mapping registers for I/O Space 1 will be enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

7. I/O WINDOW MAPPING REGISTERS

The I/O windows must never include 3E0h and 3E1h.

7.1 I/O Window Control

Register Name: **I/O Window Control** *Register Per:* socket
Index: **07h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Timing Register Select 1	*Compatibility Bit*	Auto-Size I/O Window 1	I/O Window 1 Size	Timing Register Select 0	*Compatibility Bit*	Auto-Size I/O Window 0	I/O Window 0 Size
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0 — I/O Window 0 Size

0	8-bit data path to I/O Window 0.
1	16-bit data path to I/O Window 0.

When bit 1 below is '0', this bit determines the size of the data path to I/O Window 0. When bit 1 is '1', this bit is ignored.

Bit 1 — Auto-Size I/O Window 0

0	I/O Window 0 Size (see bit 0 above) determines the data path to I/O Window 0.
1	The data path to I/O Window 0 will be determined based on -IOIS16 returned by the card.

This bit determines the data path to I/O Window 0. Note that when this bit is '1', the -IOIS16 signal (see page 17) determines the width of the data path to the card.

Bit 3 — Timing Register Select 0

0	Accesses made with timing specified in Timing Set 0.
1	Accesses made with timing specified in Timing Set 1.

This bit determines the access timing specification for I/O Window 0 (see page 72).

Bit 4 — I/O Window 1 Size

0	8-bit data path to I/O Window 1.
1	16-bit data path to I/O Window 1.

When bit 5 below is '0', this bit determines the size of the data path to I/O Window 1. When bit 5 is '1', this bit is ignored.

Bit 5 — Auto-Size I/O Window 1

0	I/O Window 1 Size (see bit 4) determines the data path to I/O Window 1.
1	The data path to I/O Window 1 will be determined based on -IOIS16 returned by the card.

This bit determines the width of the data path to I/O Window 1. Note that when this bit is '1', the -IOIS16 signal (see page 17) determines the window size. This bit must be set for proper ATA mode operation (see Chapter 11).

Bit 7 — Timing Register Select 1

0	Accesses made with timing specified in Timing Set 0.
1	Accesses made with timing specified in Timing Set 1.

This bit determines the access timing specification for I/O Window 1 (see page 72).

7.2 System I/O Map 0–1 Start Address Low

Register Name: **System I/O Map 0–1 Start Address Low** *Register Per:* socket
Index: **08h, 0Ch** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 7:0							
RW:00000000							

There are two separate System I/O Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	System I/O Map Start Address Low
8h	System I/O Map 0 Start Address Low
Ch	System I/O Map 1 Start Address Low

Bits 7:0 — Start Address 7:0

This register contains the least-significant byte of the address that specifies the beginning of the I/O space within the corresponding I/O map. I/O accesses that are equal or above this address and equal or below the corresponding System I/O Map End Address will be mapped into the I/O space of the corresponding PC Card.

The most-significant byte is located in the **System I/O Map 0–1 Start Address High** register (see page 50).

7.3 System I/O Map 0–1 Start Address High

Register Name: **System I/O Map 0–1 Start Address High** *Register Per:* socket
Index: **09h, 0Dh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 15:8							
RW:00000000							

There are two separate System I/O Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index	System I/O Map Start Address High
9h	System I/O Map 0 Start Address High
Dh	System I/O Map 1 Start Address High

Bits 15:8 — Start Address 15:8

This register contains the most-significant byte of the Start Address. See the description of the Start Address field associated with bits 7:0 of the **System I/O Map 0–1 Start Address Low** register.

7.4 System I/O Map 0–1 End Address Low

Register Name: **System I/O Map 0–1 End Address Low**							*Register Per:* socket
Index: **0Ah, 0Eh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 7:0							
RW:00000000							

There are two separate System I/O Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	System I/O Map End Address Low
Ah	System I/O Map 0 End Address Low
Eh	System I/O Map 1 End Address Low

Bits 7:0 — End Address 7:0

This register contains the least-significant byte of the address that specifies the termination of the I/O space within the corresponding I/O map. I/O accesses that are equal or below this address and equal or above the corresponding System I/O Map Start Address will be mapped into the I/O space of the corresponding PC Card.

The most-significant byte is located in the **System I/O Map 0–1 End Address High** register (see page 51).

7.5 System I/O Map 0–1 End Address High

Register Name: **System I/O Map 0–1 End Address High**							*Register Per:* socket
Index: **0Bh, 0Fh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 15:8							
RW:00000000							

There are two separate System I/O Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index	System I/O Map End Address High
Bh	System I/O Map 0 End Address High
Fh	System I/O Map 1 End Address High

Bits 15:8 — End Address 15:8

This register contains the most-significant byte of the End Address. See the description of the End Address field associated with bits 7:0 of the **System I/O Map 0–1 End Address Low** register (see page 51).

7.6 Card I/O Map 0–1 Offset Address Low

Register Name: **Card I/O Map 0–1 Offset Address Low**							*Register Per:* socket
Index: **36h, 38h**							*Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 7:1							*0*[a]
RW:0000000							RW:0

[a] This bit must be programmed to '0'.

There are two separate Card I/O Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	Card I/O Map Offset Address Low
36h	Card I/O Map 0 Offset Address Low
38h	Card I/O Map 1 Offset Address Low

Bits 7:1 — Offset Address 7:1

This register contains the least-significant byte of the quantity that will be added to the host I/O address; this will determine the PC Card I/O map location where the I/O access will occur.

The most-significant byte is located in the **Card I/O Map 0–1 Offset Address High** register (see page 52).

7.7 Card I/O Map 0–1 Offset Address High

Register Name: **Card I/O Map 0–1 Offset Address High**							*Register Per:* socket
Index: **37h, 39h**							*Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 15:8							
RW:00000000							

There are two separate Card I/O Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index	Card I/O Map Offset Address High
37h	Card I/O Map 0 Offset Address High
39h	Card I/O Map 1 Offset Address High

Bits 15:8 — Offset Address 15:8

This register contains the most-significant byte of the Offset Address. See the description of the End Address field associated with bits 7:1 of the **Card I/O Map 0–1 Offset Address Low** register (see page 52).

8. MEMORY WINDOW MAPPING REGISTERS

The following information about the memory map windows is important:

- The memory window mapping registers determine where in the ISA memory space and PC Card memory space accesses will occur. There are five memory windows that can be used independently.
- The memory windows are enabled and disabled using the **Mapping Enable** register (see page 47).
- To specify where in the ISA space a memory window is mapped, start and end addresses are specified. A memory window is selected whenever the appropriate Memory Map Enable bit (see page 47) is set, and when the ISA address is greater than or equal to the appropriate **System Memory Map Start Address** register (see page 53) and the ISA address is less than or equal to the appropriate **System Memory Map End Address** register (see page 54).
- Start and end addresses are specified with ISA Address bits 23:12. This sets the minimum size of a memory window to 4K bytes. Memory windows are specified in the ISA address from 64K bytes to 16 Mbytes (0010000h–FFFFFFh). Note that no memory window can be mapped in the first 64K bytes of the ISA address space.
- To ensure proper operation, none of the windows can overlap in the ISA address space.

8.1 System Memory Map 0–4 Start Address Low

Register Name: **System Memory Map 0–4 Start Address Low** *Register Per:* socket
Index: **10h, 18h, 20h, 28h, 30h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 19:12							
RW:00000000							

There are five separate System Memory Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	System Memory Map Start Address Low
10h	System Memory Map 0 Start Address Low
18h	System Memory Map 1 Start Address Low
20h	System Memory Map 2 Start Address Low
28h	System Memory Map 3 Start Address Low
30h	System Memory Map 4 Start Address Low

Bits 7:0 — Start Address 19:12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will begin. Memory accesses that are equal or above this address and equal or below the corresponding System Memory Map End Address will be mapped into the memory space of the corresponding PC Card.

The most-significant four bits are located in the **System Memory Map 0–4 Start Address High** register (see page 54).

8.2 System Memory Map 0–4 Start Address High

Register Name: **System Memory Map 0–4 Start Address High** *Register Per:* socket
Index: **11h, 19h, 21h, 29h, 31h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Window Data Size	*Compatibility Bit*	*Scratchpad Bits*		Start Address 23:20			
RW:0	RW:0	RW:00		RW:0000			

There are five separate System Memory Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index	System Memory Map Start Address High
11h	System Memory Map 0 Start Address High
19h	System Memory Map 1 Start Address High
21h	System Memory Map 2 Start Address High
29h	System Memory Map 3 Start Address High
31h	System Memory Map 4 Start Address High

Bits 3:0 — Start Address 23:20

This field contains the most-significant four bits of the Start Address. See the description of the Start Address field associated with bits 7:0 of the **System Memory Map 0–4 Start Address Low** register (see page 53).

Bit 7 — Window Data Size

0	8-bit data path to the card.
1	16-bit data path to the card.

This bit determines the data path size to the card.

8.3 System Memory Map 0–4 End Address Low

Register Name: **System Memory Map 0–4 End Address Low** *Register Per:* socket
Index: **12h, 1Ah, 22h, 2Ah, 32h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 19:12							
RW:00000000							

There are five separate System Memory Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	System Memory Map End Address Low
12h	System Memory Map 0 End Address Low
1Ah	System Memory Map 1 End Address Low
22h	System Memory Map 2 End Address Low
2Ah	System Memory Map 3 End Address Low
32h	System Memory Map 4 End Address Low

Bits 7:0 — End Address 19:12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will end. Memory accesses that are equal or below this address and equal or above the corresponding System Memory Map Start Address will be mapped into the memory space of the corresponding PC Card.

The most-significant four bits are located in the **System Memory Map 0–4 End Address High** register (see below).

8.4 System Memory Map 0–4 End Address High

Register Name: **System Memory Map 0–4 End Address High** *Register Per:* socket
Index: **13h, 1Bh, 23h, 2Bh, 33h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Card Timer Select		*Scratchpad Bits*		End Address 23:20			
RW:00		RW:00		RW:0000			

There are five separate System Memory Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index	System Memory Map End Address High
13h	System Memory Map 0 End Address High
1Bh	System Memory Map 1 End Address High
23h	System Memory Map 2 End Address High
2Bh	System Memory Map 3 End Address High
33h	System Memory Map 4 End Address High

Bits 3:0 — End Address 23:20

This field contains the most-significant four bits of the End Address. See the description of the End Address field associated with bits 7:0 of the **System Memory Map 0–4 End Address Low** register (see page 54).

Bits 7:6 — Card Timer Select

00	Selects Timer Set 0.
01	Selects Timer Set 1.
10	Selects Timer Set 1.
11	Selects Timer Set 1.

This field selects the timer set. Timer Set 0 and 1 reset to values compatible with standard ISA and three-wait-state cycles (see page 72).

8.5 Card Memory Map 0–4 Offset Address Low

Register Name: **Card Memory Map 0–4 Offset Address Low**							*Register Per:* socket
Index: **14h, 1Ch, 24h, 2Ch, 34h**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 19:12							
RW:00000000							

There are five separate Card Memory Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index	Card Memory Map Offset Address Low
14h	Card Memory Map 0 Offset Address Low
1Ch	Card Memory Map 1 Offset Address Low
24h	Card Memory Map 2 Offset Address Low
2Ch	Card Memory Map 3 Offset Address Low
34h	Card Memory Map 4 Offset Address Low

Bits 7:0 — Offset Address 19:12

This register contains the least-significant byte of the quantity that will be added to the host memory address that will determine where in the PC Card's memory map the memory access will occur.

The most-significant six bits are located in the **Card Memory Map 0–4 Offset Address High** register (see page 56).

8.6 Card Memory Map 0–4 Offset Address High

Register Name: **Card Memory Map 0–4 Offset Address High**							*Register Per:* socket
Index: **15h, 1Dh, 25h, 2Dh, 35h**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Write Protect	REG Setting	Offset Address 25:20					
RW:0	RW:0	RW:000000					

There are five separate Card Memory Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index	Card Memory Map Offset Address High
15h	Card Memory Map 0 Offset Address High
1Dh	Card Memory Map 1 Offset Address High
25h	Card Memory Map 2 Offset Address High
2Dh	Card Memory Map 3 Offset Address High
35h	Card Memory Map 4 Offset Address High

Bits 5:0 — Offset Address 25:20

This field contains the most-significant six bits of the Offset Address. See the description of the Offset Address field associated with bits 7:0 of the **Card Memory Map 0–4 Offset Address Low** register (see page 56).

Bit 6 — REG Setting

0	-REG (see page 16) is not active for accesses made through this window.
1	-REG is active for accesses made through this window.

This bit determines whether -REG (see page 16) will be active for accesses made through this window. Card Information Structure (CIS) memory is accessed by setting this bit to '1'.

Bit 7 — Write Protect

0	Writes to the card through this window are allowed.
1	Writes to the card through this window are inhibited.

This bit determines whether writes to the card through this window are allowed. This bit only applies to Memory Card Interface mode.

Note that this bit must be set to '0' and a memory card's 'WP' switch must be turned off to allow writes to a card using a memory interface, such as an SRAM card.

9. EXTENSION REGISTERS

9.1 Misc Control 1

Register Name: **Misc Control 1** *Index:* **16h**						*Register Per:* socket *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Inpack Enable	*Scratchpad Bits*		Speaker Enable	Pulse System IRQ	Pulse Management Interrupt	V_{CC} 3.3V	*Reserved*[a]
RW:0	RW:00		RW:0	RW:0	RW:0	RW:0	R:X W:0

[a] May be used on some versions of the CL-PD672X to read levels of the A_GPSTB and B_GPSTB pins. Contact Cirrus Logic for more information.

Bit 1 — V_{CC} 3.3V

0	-VCC_5 activated when card power is to be applied.
1	-VCC_3 activated when card power is to be applied.

This bit determines which output pin is to be used to enable V_{CC} power to the socket when card power is to be applied; it is used in conjunction with bits 5:4 of the **Power Control** register (see page 40).

Bit 2 — Pulse Management Interrupt

0	Card status change management interrupts are passed to the appropriate IRQ[XX] or -INTR pin as level-sensitive.
1	When a card status change management interrupt occurs, the appropriate IRQ[XX] or -INTR pin is driven with the pulse train shown in Figure 9-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] or -INTR pin being used for card status change management interrupts (see page 14). Note that a clock must be present on the incoming CLK for pulsed interrupts to work.

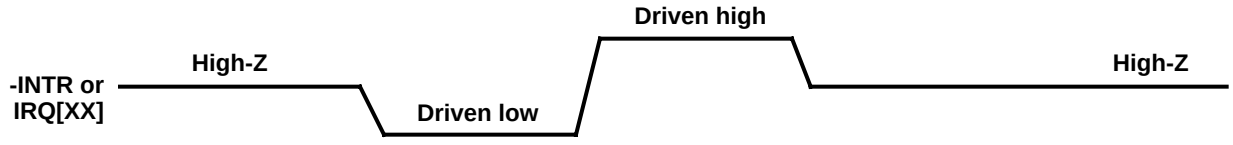


Figure 9-1. Pulse Mode Interrupts

Bit 3 — Pulse System IRQ

0	RDY/-IREQ generated interrupts are passed to the IRQ[XX] pin as level-sensitive.
1	When a RDY/-IREQ interrupt occurs, the IRQ[XX] pin is driven with the pulse train shown in Figure 9-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] pins for interrupts from a PC Card's RDY/-IREQ pin (see page 13).

Bit 4 — Speaker Enable

0	SPKR_OUT* is high-impedance.
1	SPKR_OUT* is driven from the XOR of -SPKR from each enabled socket.

This bit determines whether the card -SPKR pin will drive SPKR_OUT* (see page 15).

Bit 7 — Inpack Enable

0	-INPACK pin (see page 17) ignored.
1	-INPACK pin used to control data bus drivers during I/O read from the socket.

This bit is used to determine when to drive data onto the ISA bus.

9.2 FIFO Control

Register Name: **FIFO Control** *Index:* **17h**							*Register Per:* socket *Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Empty Write FIFO	*Scratchpad Bits*[a]						
RW	RW:0000000						

[a] Because a write will fush the FIFO, these scratchpad bits should be used only when card activity is guaranteed not to occur.

Bit 7 — Empty Write FIFO

Value	I/O Read	I/O Write
0	FIFO not empty	No operation occurs; default on reset
1	FIFO empty	Flush the FIFO

This bit controls FIFO operation and reports FIFO status. When this bit is written to '1', all data in the FIFO is lost. During read operations when this bit is '1', the FIFO is empty. During read operations when this bit is '0', data is still in the FIFO. This bit is used to ensure the FIFO is empty before changing timing registers.

FIFO contents will be lost whenever any of the following occur:

- PWRGOOD pin (see page 13) is '0'.
- The card is removed.
- V_{CC} Power bit (see page 41) is programmed to '0'.

9.3 Misc Control 2

Register Name: **Misc Control 2** *Index:* **1Eh**						*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
IRQ15 Is RI Out	DMA System *(CL-PD6712/ CL-PD6722)*	Three-State Bit 7	Drive LED Enable	5V Core	Suspend	Low-Power Dynamic Mode	Bypass Frequency Synthesizer
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:1	RW:0

Bit 0 — Bypass Frequency Synthesizer

0	Normal operation, internal clock = CLK input frequency x 7/4.
1	Internal clock = CLK input frequency (see page 15).

This bit determines internal time base.

Bit 1 — Low-Power Dynamic Mode

0	Clock runs always.
1	Normal operation, stop clock when possible.

This bit determines whether Low-Power Dynamic mode is enabled. For maximum operational power savings, keep this bit set to '1'.

Bit 2 — Suspend

0	Normal operation.
1	Stop Frequency Synthesizer, enable all Low-Power modes and disable socket access.

This bit enables Suspend mode. After entering Suspend, AEN should be pulled high for lowest power consumption. When this bit is high and AEN is high, all ISA bus interface inputs are turned off. In 82386SL systems when the processor is in Suspend mode, the ISA bus interface signals float; this feature will prevent high current flow in the CL-PD67XX inputs.

Bit 3 — 5V Core

0	Normal operation: use when CORE_VDD pin is connected to 3.3 volts.
1	Selects input thresholds for use when 5.0 volts is connected to the CL-PD67XX CORE_VDD pins.

This bit selects input threshold circuits for use when 3.3 or 5.0 volts is connected to the CL-PD67XX CORE_VDD pins. This bit must be set to '0' when the CORE_VDD pins are connected to 3.3 volts to preserve TTL-compatible input thresholds to the card socket.

Bit 4 — Drive LED Enable

0	IRQ12 operates normally.
1	IRQ12 becomes an open-drain output suitable for driving an LED (driven whenever the card -SPKR output is turned on, and the corresponding Speaker Is LED input bit (see page 64) is set).

NOTE: This bit should be set to '0' if in Memory Card Interface mode.

This bit determines whether -SPKR is used to drive an LED on the IRQ12 (see page 14) for disk drives.

Bit 5 — Three-State Bit 7

0	Normal operation.
1	For socket I/O at address 03F7h and 0377h, do not drive bit 7.

This bit enables floppy change bit compatibility.

Bit 6 — DMA System (CL-PD6712 and CL-PD6722 only)

0	Configured for non-DMA mode on theCL-PD6712 and CL-PD6722.
1	Configured for DMA mode on the CL-PD6712 and CL-PD6722.

This bit is reserved for the CL-PD6720.

On the CL-PD6712 and CL-PD6722, this bit is used to configure system interface signals for normal or DMA operation. At reset, the signals IRQ9, IRQ10, and -VPP_VALID are in non-DMA mode, and this bit is set to '0'. When this bit is set to '1', the IRQ9, IRQ10, and -VPP_VALID pins are reconfigured for system bus DMA interfacing. Refer to Chapter 14 for a functional description of these pins during DMA operation.

Bit 7 — IRQ15 Is RI Out

0	Normal IRQ15 operation.
1	IRQ15 is connected to Ring Indicate pin on the host processor.

This bit determines the function of the IRQ15 pin. When configured for ring indicate, IRQ15 is used to resume a processor with NMI or SMI such as an 82486SL when a high-to-low change is detected on the -STSCHG pin.

9.4 Chip Information

Register Name: **Chip Information** *Register Per:* chip
Index: **1Fh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Cirrus Logic Host-Adapter Identification		Dual/Single Socket*	CL-PD67XX Revision Level				*Reserved*
R:11		R:n[a]	R:nnnn[b]				R:n[c]

[a] The value for CL-PD6712 is '0', and the value for CL-PD6720 and CL-PD6722 is '1'.

[b] This read-only value depends on the revision level of the CL-PD67XX chip.

[c] The value for CL-PD6720 is '0', and the value for CL-PD6712 and CL-PD6722 is '1'.

Bits 4:1 — CL-PD67XX Revision Level

This field identifies the revision of the controller. The initial value is '111'. Contact Cirrus Logic for more information on revision levels for the CL-PD6712, CL-PD6720, and CL-PD6722.

Bit 5 — Dual/Single Socket*

0	Chip identified as a single-socket controller.
1	Chip identified as a dual-socket controller.

This bit specifies the number of sockets supported by the CL-PD67XX.

Bits 7:6 — Cirrus Logic Host-Adapter Identification

00	Second read after I/O write to this register.
11	First read after I/O write to this register.

This field identifies a Cirrus Logic host-adapter device. After chip reset or doing an I/O write to this register, the first read of this register will return '11'. On the next read, this field will be '00'. This pattern of toggling data on subsequent reads can be used by software to determine presence of a Cirrus Logic host adapter in a system or to determine occurrence of a device reset.

9.5 ATA Control

Register Name: **ATA Control** *Index:* **26h**						*Register Per:* socket *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
A25/CSEL	A24/M/S*	A23/VU	A22	A21	*Scratchpad Bit*	Speaker Is LED Input	ATA Mode
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0 — ATA Mode

0	Normal operation.
1	Configures the socket interface to handle ATA-type disk drives.

This bit reconfigures the particular socket as an ATA drive interface. Refer to Table 11-1 on page 75 for PC Card socket pin definitions in ATA mode.

Bit 1 — Speaker Is LED Input

0	Normal operation.
1	The PC Card -SPKR pin will be used to drive IRQ12 if Drive LED Enable (see page 61) is set.

This bit changes the function of the BVD2/-SPKR/-LED pin (see page 18) from digital speaker input to disk status LED input. When in I/O Card Interface mode or ATA mode, setting this bit to '1' reconfigures the BVD2/-SPKR/-LED input pin to serve as a -LED input from the socket.

NOTE: This bit should be set to '0' if in Memory Card Interface mode.

Bit 3 — A21

In ATA mode, the value in this bit is applied to the ATA A21 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PC Card Standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 4 — A22

In ATA mode, the value in this bit is applied to the ATA A22 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PC Card Standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 5 — A23/VU

In ATA mode, the value in this bit is applied to the ATA A23 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PC Card Standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 6 — A24/M/S*

In ATA mode, the value in this bit is applied to the ATA A24 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PC Card Standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 7 — A25/CSEL

In ATA mode, the value in this bit is applied to the ATA A25 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PC Card Standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

9.6 Extended Index

Register Name: **Extended Index** *Register Per:* socket
Index: **2Eh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Extended Index							
RW:00000000							

This register controls which of the following registers at index 2Fh can be accessed:

Register Name at Index 2Fh	Extended Register Index
Scratchpad	00h
Data Mask 0	01h
Data Mask 1	02h
Extension Control 1 (formerly named DMA Control)	03h
Maximum DMA Acknowledge Delay	04h
Reserved	05h–09h
External Data	0Ah
Extension Control 2	0Bh

9.7 Extended Data

Register Name: **Extended Data** *Register Per:* socket
Index: **2Fh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Extended Data							

The data in this register allows the registers indicated by the **Extended Index** register to be read and written. The value of this register is the value of the register selected by the **Extended Index** register.

9.7.1 Data Mask 0–1

Register Name: **Data Mask 0–1** *Register Per:* socket
Index: **2Fh** *Extended Index:* **01h, 02h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Data Mask Select 0–1							
RW:00000000							

Data Mask 0 is the mask register for I/O Map 0. For each bit set in the Data Mask Select 0 field, the corresponding data bit will not be driven when the host addresses PC Card I/O addresses in the I/O Map 0

range. If this register is set to 00h, then all data bits will be driven from the PC Card to the ISA bus (this is the reset condition). If any bits are set to '1', accesses to the I/O Map 0 range of I/O on the PC Card will be forced to 8-bit operation on the ISA side. If, for example, I/O Map 0 registers are set for the range 3F7h to 3F7h, I/O Map 1 registers are set for the range 3F0h to 3F6h, Data Mask Select 0 is set to 7Fh, and a floppy drive is the PC Card device, then the conflict between the floppy address 3F7h and the hard disk register at 3F7h would not cause a conflict on the ISA bus — the floppy change bit would be correctly presented to the host.

The **Data Mask 1** register operates the same as the **Data Mask 0** register but acts on I/O addresses in the range indicated by the I/O Map 1 registers.

9.7.2 Extension Control 1 (formerly named DMA Control)

Register Name: **Extension Control 1** *Register Per:* socket
Index: **2Fh** *Extended Index:* **03h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
DMA Enable *(CL-PD6712/CL-PD6722)*		Pull-up Control	*Reserved*		LED Activity Enable	Auto Power Clear Disable	V_{CC} Power Lock
RW:00		RW:0	RW:00		RW:0	RW:0	RW:0

Bit 0 — V_{CC} Power Lock

0	The V_{CC} Power bit (bit 4 of **Power Control** register) is not locked.
1	The V_{CC} Power bit (bit 4 of **Power Control** register) cannot be changed by software.

This bit can be used to prevent card drivers from overriding the Socket Services' task of controlling power to the card, thus preventing situations where cards are powered incorrectly.

Bit 1 — Auto Power Clear Disable

0	The V_{CC} Power bit (bit 4 of **Power Control** register) is reset to '0' when the card is removed.
1	The V_{CC} Power bit (bit 4 of **Power Control** register) is not affected by card removal.

Bit 2 — LED Activity Enable

0	LED activity disabled.
1	LED activity enabled.

This bit allows the LED_OUT* pin to reflect any activity in the card. Whenever PC Card cycles are in process to or from a card in either socket, LED_OUT* will be active (low).

Bit 5 — Pull-up Control

0	Pull-ups on CD2, CD1, and VS1#/A_GPSTB and VS2#/B_GPSTB (CL-PD6712) or A_GPSTB and B_GPSTB (CL-PD672X) are in use.
1	Pull-ups on CD2, CD1, and VS1#/A_GPSTB and VS2#/B_GPSTB (CL-PD6712) or A_GPSTB and B_GPSTB (CL-PD672X) are turned off.

This bit turns off the pull-ups on CD2, CD1, and VS1#/A_GPSTB and VS2#/B_GPSTB (CL-PD6712) or A_GPSTB and B_GPSTB (CL-PD672X). Turning off these pull-ups can be used in addition to Suspend mode to even further reduce power when cards are inserted but no card accessibility is required. Even though power may or may not still be applied, all pull-ups and their associated inputs will be disabled.

Note that insertion or removal of a card or sensing of a card's voltage range (CL-PD6712) cannot be determined when this bit is set to '1'. Also, if card detect interrupts are enabled and a card is already in the socket, a card detect interrupt will be generated when this bit is changed.

Bit 7:6 — DMA Enable (CL-PD6712 and CL-PD6722 only)

On the CL-PD6712 and CL-PD6722, DMA Enable bits 6 and 7 enable the DMA operation of the PC Card socket. At reset these bits are set to '0', and this is non-DMA mode. If either or both of these bits is set, the socket is in DMA mode. The three codes that cause DMA mode also select the use of one of three pins for the active-low -DREQ input at the PC Card interface.

Bit 7	Bit 6	Pin Used
0	1	-INPACK
1	0	WP/-IOIS16
1	1	BVD2/-SPKR

For cards requiring DMA services but also needing input acknowledge functionality, or needing to indicate the size of I/O registers within a window, or needing digital speaker or LED operation, the selection of the -DREQ signal to the socket is made to be as flexible as possible.

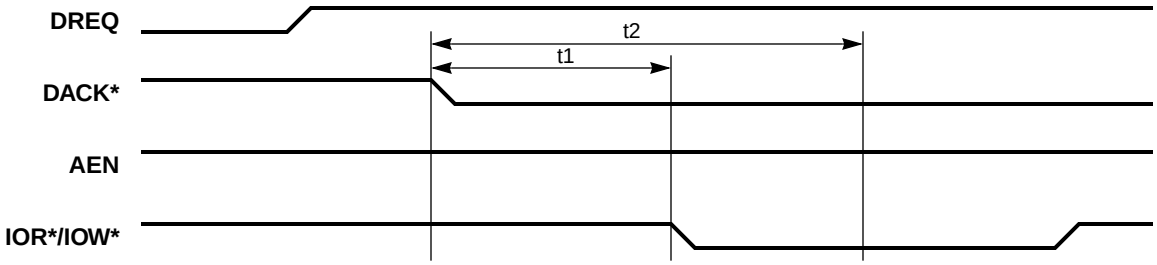
9.7.3 Maximum DMA Acknowledge Delay (CL-PD6712 and CL-PD6722 only)

Register Name: **Maximum DMA Acknowledge Delay** — *Register Per:* socket
Index: **2Fh** — *Extended Index:* **04h** — *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Maximum DMA Acknowledge Delay							
RW:00000000							

During a DMA data transfer process, an ISA-based system typically follows its issuance of a DMA acknowledge with a DMA read or write cycle. However, during a DMA write-verify operation, a system can issue a DMA acknowledge without following it with a DMA read or write cycle. Because a DMA-capable PC Card receives DMA acknowledgment only by reception of a DMA read or write cycle, conditions may occur where the card never receives a DMA acknowledge. To prevent this from happening in an ISA-based system, a maximum DMA acknowledge delay feature has been added that generates a 'dummy' DMA write cycle (reads DMA data from the card) if there are no system-generated DMA read or write cycles to the card within a programmable time.

Once a DMA acknowledge is received from the system, the CL-PD6712 or CL-PD6722 starts counting the time from the assertion of the DACK* signal until the system issues a DMA read or write command (IOR* or IOW*). If this interval exceeds the programmed time, the CL-PD6712 or CL-PD6722 assumes that a system write-verify is in progress and generates a dummy DMA write cycle at the PC Card interface. This allows the passing of the DMA acknowledge (and terminal count status) to the card so it can perform any intended verify-cycle functions.



t1 = time delay from DMA acknowledge to IOR* or IOW* command (specified by system design).
t2 = time to program into the Maximum DMA Acknowledge Delay register for when IOR* or IOW* falling edge does not occur (t2 > t1).

Figure 9-2. Selection of Acknowledge Time-out Interval

The maximum DMA acknowledge delay (t2 as shown in Figure 9-2) should be programmed to a time greater than the maximum time required from the system's issuance of a DMA acknowledge to its issuance of a DMA read or write cycle (t1 as shown in Figure 9-2). The t1 time is indicated in the specifications for the systems DMA cycle timing.

Typical system specifications for t1 are 190–270 ns, making a value of 80h for the **Maximum DMA Acknowledge Delay** register suitable for many applications. If the CL-PD6712 or CL-PD6722 is used in an add-in card application, a value of 20h may be suitable. Table 9-1 shows **Maximum DMA Acknowledge Delay** register values to be programmed for a desired maximum DMA acknowledge delay.

Table 9-1. Maximum DMA Acknowledge Delay Register Values

Register Value	Maximum DMA Acknowledge Delay (25-MHz internal clock and default Setup timing)
80h	7 clocks = 280 ns
40h	8 clocks = 320 ns
C0h	9 clocks = 360 ns
20h	10 clocks = 400 ns
A0h	11 clocks = 440 ns
60h	12 clocks = 480 ns
E0h	13 clocks = 520 ns
10h	14 clocks = 560 ns
90h	15 clocks = 600 ns
50h	16 clocks = 640 ns
D0h	17 clocks = 680 ns
30h	18 clocks = 720 ns
B0h	19 clocks = 760 ns

9.7.4 External Data (Socket A, Index 2Fh)

Register Name: **External Data**			*Extended Index:* **0Ah**			*Register Per:* socket	
Index: **2Fh only**						*Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
External Data 7	External Data 6	External Data 5	External Data 4	External Data 3	External Data 2	External Data 1	External Data 0
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bits 7:0 — External Data

This register is updated and accessed according to the setting of bits 3 and 4 of the Socket A **Extension Control 2** register (Index 2Fh, Extended Index 0Bh).

Table 9-2. Functions of Socket A External Data Register

Socket A Extension Control 2		Function of Socket A External Data Register
Bit 4: GPSTB on IOW*	**Bit 3: GPSTB on IOR***	
0	0	Scratchpad
0	1	External read port: A_GPSTB is a read buffer enable for external data on SD[15:8]
1	0	External write port: A_GPSTB is a write latch enable for SD[15:8] to get latched to an external register. Reads of Socket A External Data register produce the value written to the latch.
1	1	Reserved

NOTE: For software compatibility of external data access accross the Cirrus Logic PC Card host adapter product line, the Socket A **External Data** register should only be used as a *write* port and not as a *read* port. Also for compatibility, only the lower nibble of **External Data** should be accessed and the upper nibble should be ignored.

Refer to Chapter 12 for more information on the use of the **External Data** register.

9.7.5 External Data (Socket A, Index 6Fh)

Register Name: **External Data**							*Register Per:* socket
Index: **6Fh only**			*Extended Index:* **0Ah**				*Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
External Data 7	External Data 6	External Data 5	External Data 4	External Data 3 or B_VS2# Input	External Data 2 or B_VS1# Input	External Data 1 or A_VS2# Input	External Data 0 or A_VS1# Input
RW:0	RW:0	RW:0	RW:0	R:0	R:0	R:0	R:0

Bits 7:0 — External Data

This register is updated and accessed according to the setting of bits 3 and 4 of the Socket B **Extension Control 2** register (Index 6Fh, Extended Index 0Bh).

Table 9–3. Functions of Socket B External Data Register

Socket B Extension Control 2		Function of Socket B External Data Register
Bit 4: GPSTB on IOW*	**Bit 3: GPSTB on IOR***	
0	0	Bits 7:4 — scratchpad Bits 3:2 — Socket B VS2# and VS1# levels (CL-PD672X only) Bits 1:0 — Socket A VS2# and VS1# levels
0	1	External read port: B_GPSTB is a read buffer enable for external data on SD[15:8]
1	0	External write port: B_GPSTB is a write latch enable for SD[15:8] to get latched to an external register. Reads of Socket B External Data register produce the value written to the latch.
1	1	Reserved

NOTE: For software compatibility of external data access accross the Cirrus Logic PC Card host adapter product line, the Socket B **External Data** register should only be used as a *read* port and not as a *write* port. Also for compatibility, only the lower nibble of **External Data** should be accessed and the upper nibble should be ignored. For software compatibility with VS1# and VS2# detection software, when Socket B is used as a read port, socket VS1# and VS2# signals should be connected to the external read buffer as shown in Figure 13-2.

Refer to Chapter 12 for more information on the use of the **External Data** register, and Chapter 13 for more information on VS1# and VS2# detection.

9.7.6 Extension Control 2

Register Name: **Extension Control 2**						*Register Per:* socket	
Index: **2Fh**			*Extended Index:* **0Bh**			*Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved		Active-high GPSTB	GPSTB on IOW*	GPSTB on IOR*	Totem-pole GPSTB	*Reserved*	
RW:00		RW:0	RW:0	RW:0	RW:0	RW:00	

Bit 5 — Active-high GPSTB

0	GPSTB ouputs are active-low.
1	GPSTB ouputs are active-high.

Bit 4 — GPSTB on IOW*

0	VS1#/A_GPSTB (CL-PD6712) or A_GPSTB (CL-PD672X) pins are used as voltage sense.
1	VS1#/A_GPSTB (CL-PD6712) or A_GPSTB (CL-PD672X) pins are used to strobe I/O writes on SD[15:8].

Note that setting this bit forces the pull-ups on VS1#/A_GPSTB (CL-PD6712) and A_GPSTB (CL-PD672X) to be off, independent of the setting of the Pull-Up Control bit (index 2Fh, extended index 03h, bit 5). See Section 9.7.5, Chapter 12, and Chapter 13.

Bit 3 — GPSTB on IOR*

0	VS2#/B_GPSTB (CL-PD6712) or B_GPSTB (CL-PD672X) pins (socket B) are used as voltage sense.
1	VS2#/B_GPSTB (CL-PD6712) or B_GPSTB (CL-PD672X) pins are used to strobe I/O reads on SD[15:8].

Note that setting this bit forces the pull-ups on VS2#/B_GPSTB (CL-PD6712) or B_GPSTB (CL-PD672X) to be off, independent of the setting of the Pull-Up Control bit (index 6Fh, extended index 03h, bit 5). See Section 9.7.5, Chapter 12, and Chapter 13.

Bit 2 — Totem-pole GPSTB

0	GPSTB ouputs are open-collector.
1	GPSTB ouputs are totem-pole.

When GPSTB outputs are totem-pole, their 'high' level is driven to the level of the +5V pin, instead of high-impedance.

10. TIMING REGISTERS

The following information about the timing registers is important:

- All timing registers take effect immediately and should only be changed when the FIFO is empty (see the **FIFO Control** register on page 60).
- Selection of Timing 0 or Timing 1 register sets is controlled by **I/O Window Control**, bit 3 and/or bit 7 (see page 49).

10.1 Setup Timing 0–1

Register Name: **Setup Timing 0–1** *Register Per:* socket
Index: **3Ah, 3Dh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Setup Prescalar Select		Setup Multiplier Value					
RW:00		RW:000001					

There are two separate Setup Timing registers, each with identical fields. These registers are located at the following indexes:

Index	Setup Timing
3Ah	Setup Timing 0
3Dh	Setup Timing 1

The Setup Timing register for each timing set controls how long a PC Card cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 16) setup will be, in terms of the number of internal clock cycles.

The overall command setup number of clocks *S* is programmed by selecting a 2-bit prescaling value (bits 7:6 of this register) representing weights of 1, 16, 256, or 8192, and then selecting a multiplier value (bits 5:0) to which that prescalar is multiplied to produce the overall command setup timing length according to the following formula:

$$S = (N_{pres} \times N_{val}) + 1 \qquad \textbf{Equation 10-1}$$

The value of *S*, representing the number of internal clock cycles for command setup, is then multiplied by the internal clock's period to determine the command setup time (see Section 15.3.6 for further discussion).

Bits 5:0 — Setup Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7:6) to control the length of setup time before a command becomes active.

Bits 7:6 — Setup Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 8192$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Setup Multiplier Value (bits 5:0) to control the length of setup time before a command becomes active.

10.2 Command Timing 0–1

Register Name: **Command Timing 0–1** *Index:* **3Bh, 3Eh**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Command Prescalar Select		Command Multiplier Value					
RW:00		RW:000110/001111[a]					

[a] Timing set 0 (index 3Bh) resets to 06h for socket timing equal to standard AT-bus-based cycle times. Timing set 1 (3Eh) resets to 0Fh for socket timings equal to standard AT-bus timing using one additional wait state.

There are two separate Command Timing registers, each with identical fields. These registers are located at the following indexes:

Index	Command Timing
3Bh	Command Timing 0
3Eh	Command Timing 1

The Command Timing register for each timing set controls how long a PC Card cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 16) active time will be, in terms of the number of internal clock cycles.

The overall command timing length *C* is programmed by selecting a 2-bit prescaling value (bits 7:6 of this register) representing weights of 1, 16, 256, or 8192, and then selecting a multiplier value (bits 5:0) to which that prescalar is multiplied to produce the overall command timing length according to the following formula:

$$C = (N_{pres} \times N_{val}) + 1 \qquad \textbf{Equation 10-2}$$

The value of *C*, representing the number of internal clock cycles for a command, is then multiplied by the internal clock's period to determine the command active time (see Section 15.3.6 for further discussion).

Bits 5:0 — Command Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7:6) to control the length that a command is active.

Bits 7:6 — Command Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 8192$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Command Multiplier Value (bits 5:0) to control the length that a command is active.

10.3 Recovery Timing 0–1

Register Name: **Recovery Timing 0–1**							*Register Per:* socket
Index: **3Ch, 3Fh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Recovery Prescalar Select		Recovery Multiplier Value					
RW:00		RW:000011					

There are two separate Recover Timing registers, each with identical fields. These registers are located at the following indexes:

Index	Recovery Timing
3Ch	Recovery Timing 0
3Fh	Recovery Timing 1

The Recovery Timing register for each timing set controls how long a PC Card cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 16) recovery will be, in terms of the number of internal clock cycles.

The overall command recovery timing length *R* is programmed by selecting a 2-bit prescaling value (bits 7:6 of this register) representing weights of 1, 16, 256, or 8192, and then selecting a multiplier value (bits 5:0) to which that prescalar is multiplied to produce the overall command recovery timing length according to the following formula:

$$R = (N_{pres} \times N_{val}) + 1 \qquad \textbf{Equation 10-3}$$

The value of *R*, representing the number of internal clock cycles for command recovery, is then multiplied by the internal clock's period to determine the command recovery time (see Section 15.3.6 for further discussion).

Bits 5:0 — Recovery Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7:6) to control the length of recovery time after a command is active.

Bits 7:6 — Recovery Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 8192$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Recovery Multiplier Value (bits 5:0) to control the length of recovery time after a command is active.

11. ATA MODE OPERATION

The CL-PD67XX PC Card interfaces can be dynamically configured to support a PC Card–compatible ATA disk interface (commonly known as 'IDE') instead of the standard PC Card interface. Disk drives that can be made mechanically-compatible with PC Card dimensions can thus operate through the socket using the ATA electrical interface.

Configuring a socket to support ATA operation changes the function of certain card socket signals to support the needs of the ATA disk interface. Table 11-1 lists each interface pin and its function when a CL-PD67XX card socket is operating in ATA mode. Refer to application note AN-PD5, *Configuring PCMCIA Sockets for ATA Drive Interface*, for more information.

All register functions of the CL-PD67XX are available in ATA mode, including socket power control, interface signal disabling, and card window control. No memory operations are allowed in ATA mode.

Table 11-1. ATA Pin Cross-reference

PC Card Socket Pin Number	Function	
	PC Card Interface	ATA Interface
1	Ground	Ground
2	D3	D3
3	D4	D4
4	D5	D5
5	D6	D6
6	D7	D7
7	-CE1	-CS0
8	A10	n/c
9	-OE	-ATA (always low)
10	A11	n/c
11	A9	CS1*
12	A8	n/c
13	A13	n/c
14	A14	n/c
15	-WE	n/c
16	-IREQ	IREQ
17	VCC	VCC
18	VPP1	n/c
19	A16	n/c
20	A15	n/c
21	A12	n/c

PC Card Socket Pin Number	Function	
	PC Card Interface	ATA Interface
35	Ground	Ground
36	-CD1	-CD1
37	D11	D11
38	D12	D12
39	D13	D13
40	D14	D14
41	D15	D15
42	-CE2	-CS1
43	VS1	VS1
44	-IORD	-IORD
45	-IOWR	-IOWR
46	A17	n/c
47	A18	n/c
48	A19	n/c
49	A20	n/c
50	A21	n/c
51	VCC	VCC
52	VPP2	n/c
53	A22	n/c
54	A23	VU
55	A24	-M/S

Table 11-1. ATA Pin Cross-reference *(cont.)*

PC Card Socket Pin Number	Function	
	PC Card Interface	ATA Interface
22	A7	n/c
23	A6	n/c
24	A5	n/c
25	A4	n/c
26	A3	n/c
27	A2	A2
28	A1	A1
29	A0	A0
30	D0	D0
31	D1	D1
32	D2	D2
33	-IOIS16	-IOIS16
34	Ground	Ground

PC Card Socket Pin Number	Function	
	PC Card Interface	ATA Interface
56	A25	CSEL
57	VS2	VS2
58	RESET	RESET*
59	-WAIT	IOCHRDY
60	-INPACK	DREQ [a]
61	-REG	-DACK [a]
62	-SPKR	-LED
63	-STSCHG	-PDIAG [a]
64	D8	D8
65	D9	D9
66	D10	D10
67	-CD2	-CD2
68	Ground	Ground

[a] Not supported by the CL-PD67XX.

12. USING GPSTB PINS FOR EXTERNAL PORT CONTROL

The CL-PD67XX provides pins that can be programmed to function as general-purpose strobes to external latches or buffers, allowing them to serve as read ports or write ports mapped into the CL-PD67XX register set.

Configuring a GPSTB pin as a read port allows an easy way to read additional card status such as VS1# and VS2# levels, a card socket microswitch status, a card port cover microswitch status, card eject solenoid position status, or general system signal status.

Configuring a GPSTB pin as a write port allows an easy way to control additional features such as card-state LED's, card mechanism solenoids, or motor eject mechanisms.

12.1 Control of GPSTB Pins

The **Extension Control 2** register controls the GPSTB pins.

For the CL-PD672X, the A_GPSTB pin is controlled by the **Extension Control 2** register at Socket A (index 2Fh, extended index 0Bh), and the B_GPSTB pin is controlled by the **Extension Control 2** register at Socket B (index 6Fh, extended index 0Bh).

For the CL-PD6712, the VS1#/A_GPSTB pin is controlled by the **Extension Control 2** register at extended index 0Bh and the VS2#/B_GPSTB pin is controlled by a 'Virtual Socket B' extended index register (index 6Fh, extended index 0Bh).

The following table summarizes how the GPSTB pins are configured and how data is accessed from external ports created by using a GPSTB pin to control an external read or write port.

Table 12-1. Registers for Control and Data of GPSTB Pins

Pin Name	GPSTB Control Access	External Port Data Access
VS1#/A_GPSTB (CL-PD6712) A_GPSTB (CL-PD672X)	Set register 2E to 0Bh, access **Extension Control 2** register at 2F	Set register 2E to 0Ah, access **External Data** register at 2F
VS2#/B_GPSTB (CL-PD6712) B_GPSTB (CL-PD672X)	Set register 6E to 0Bh, access **Extension Control 2** register at 6F	Set register 6E to 0Ah, access **External Data** register at 6F

Programming the Extension Control 2 Register

There is one **Extension Control 2** register per GPSTB pin. Each register has identical GPSTB control bits, as follows. See also the description of this register in Section 9.7.6.

Register Name: **Extension Control 2** *Register Per:* socket
Index: **2Fh and 6Fh** *Extended Index:* **0Bh** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Active-high GPSTB	GPSTB on IOW*	GPSTB on IOR*	Totem-pole GPSTB	*Reserved*	
RW:00		RW:0	RW:0	RW:0	RW:0	RW:00	

Bit 5 allows programming of the active level of GPSTB, with the default being active-low. Setting bit 5 to '1' causes a GPSTB output to be low normally and high (active) upon external data access.

Bit 4 controls use of the respective GPSTB pin as a write strobe for an external general-purpose latch. When the respective extended index is set to 0Ah and the index register is set to the respective 2Fh or 6Fh setting, I/O writes that access address 3E1h will result in the respective GPSTB signal being driven active for the duration of the ISA bus IOW* signal being driven low.

Bit 3 controls use of the respective GPSTB pin a read strobe for an external general-purpose buffer. When the respective extended index is set to 0Ah and the index register is set to the respective 2Fh or 6Fh setting, I/O reads that access address 3E1h will result in the respective GPSTB signal being driven active for the duration of the ISA bus IOR* signal being driven low.

Bit 2 cause the GPSTB output to be totem-pole instead of the default open-collector configuration. When GPSTB outputs are totem-pole, their 'high' level is driven to the voltage of the '+5V' pin, instead of to high-impedance.

If neither bit 3 nor bit 4 is set, the respective GPSTB pin functions as a reserved input in a CL-PD672X or as a VS1# or VS2# input in a CL-PD6712 with an internal pull-up to the '+5V' pin. This internal pull-up is turned off whenever the GPSTB pin is configured as a general-purpose strobe, or when the respective socket's Pull-up Control bit is set to '1'.

Bits 7:6 and 1:0 are reserved and *must* be programmed to '0'. These bits should not be used as scratch-pad bits.

External Data Port Access through the External Data Register

Data to be accessed from an external read or write port is mapped to the respective **External Data** register at Extended Index 0Ah. This allows external data to be accessed as if it were a register in the CL-PD67XX register set.

To achieve this mapping, the external data port's buffer or latch data connections should be made to SD[15:8] of the system bus for 16-bit systems, and to SD[7:0] of the system bus for 8-bit systems.

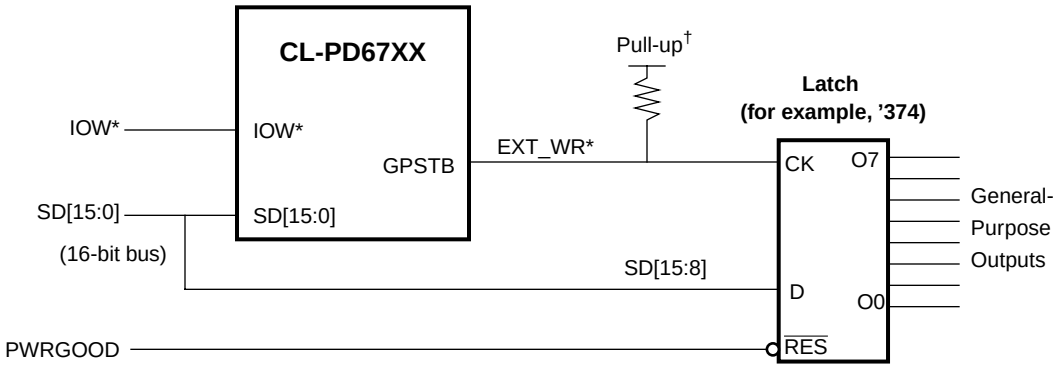
To support readback of data written to an external I/O port by use of a GPSTB pin, a shadow of the external data register exists, which is read when an I/O read is done from the external data register location corresponding to a GPSTB pin programmed as a write strobe.

For more information on the Socket A and Socket B versions of this register, see the description of this register in Section 9.7.4 and Section 9.7.5.

Register Name: **External Data** *Index:* **2Fh**			*Extended Index:* **0Ah**			*Register Per:* socket *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
External Data 7	External Data 6	External Data 5	External Data 4	External Data 3	External Data 2	External Data 1	External Data 0
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

On a CL-PD6712, bits 0 and 1 default to the VS1# /GPSTB and VS2#/B_GPSTB input levels if no GPSTB functions are programmed for the VS2#/GPSTB pin (extended index 0Bh at index 6Eh/6Fh bits 4:3 are '00'). See Chapter 13 for further explanation.

12.2 Example Implementations of GPSTB-Controlled Read and Write Ports



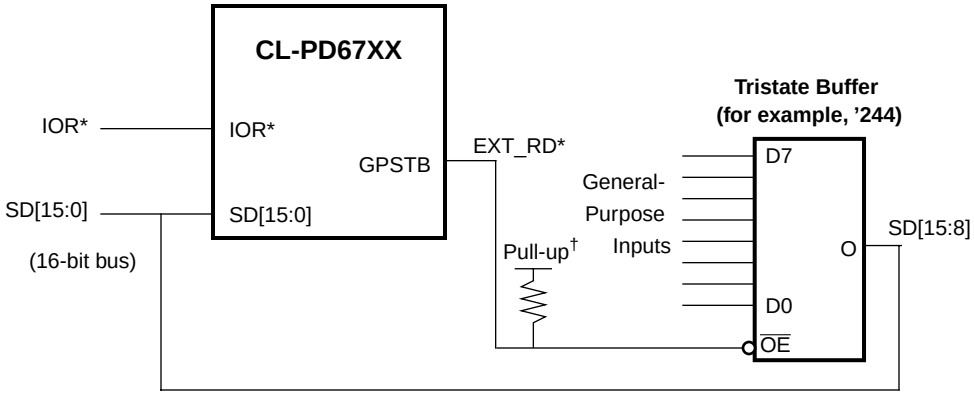
† Pull-up resistor, or set Extension Control 2 bit 2 to '1' for totem-pole output.

Figure 12-1. Example GPSTB Write Port (Extension Control 2 bits 4:3 are '10')

In this mode, **Extension Control 2** register bit 4 is set to '1' enabling the GPSTB pin to function as a write strobe. Writes to the respective extended index 0Ah cause the respective GPSTB to go active (low) for the duration of the system's IOW* pulse.

On writes, data is written to both the external latch and the internal shadow copy of the **External Data** register. A read of the respective extended index 0Ah would produce the last value written to the latch.

Connection of the ISA bus PWRGOOD signal to the external latch ensures that the latch assumes all '0's at its outputs when the CL-PD67XX is reset.



† Pull-up resistor, or set Extension Control 2 bit 2 to '1' for totem-pole output.

Figure 12-2. Example GPSTB Read Port (Extension Control 2 bits 4:3 are '01')

In this mode, **Extension Control 2** register bit 3 is set to '1', enabling the respective GPSTB pin to function as a read strobe. Reads from the corresponding extended index 0Ah cause GPSTB to go active (default active level is low) for the duration of the system's IOR* pulse.

NOTE: Data is still written to the shadowed **External Data** register on writes to Extended Index 0Ah but is not visible.

12.3 GPSTB in Suspend Mode

GPSTB read and write strobes operate while the device is in suspend mode, but they are not allowed when the device is in hardware-assisted 'Super-Suspend' mode (AEN held high while in Suspend mode).

A clock to the CL-PD672X is not required for the external signal at GPSTB to occur, but shadowing of write values in the internal register at Extended Index 0Ah requires that the CL-PD67XX is not in Suspend mode so there is an active internal clock for register writes.

13. VS1# AND VS2# VOLTAGE DETECTION

The CL-PD67XX provides support for VS1# and VS2# voltage sense for environments where special low-voltage keyed PC Card sockets are to be used. With a low-voltage keyed socket, it is necessary to determine the operating voltage range of a card before applying power to it. The CL-PD67XX supports reading of the levels on a socket's VS1# and VS2# pins through a uniform extended register programming model using Socket B extended register 0Ah. The programming model is as follows:

Register Name: **External Data** *Index:* **6Fh**			*Extended Index:* **0Ah**			*Register Per:* socket *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
External Data 7	External Data 6	External Data 5	External Data 4	B_VS2 Input	B_VS1 Input	A_VS2 Input	A_VS1 Input
RW:0	RW:0	RW:0	RW:0	R:0	R:0	R:0	R:0

On the CL-PD6712, the socket's VS1# and VS2# pins can be directly connected to the VS1#/GPSTB and VS2#/B_GPSTB pins. No **Extension Control 2** register programming is done in this case and the VS1 and VS2 bits appear as bits 0 and 1 of extended register 0Ah at index 6Fh.

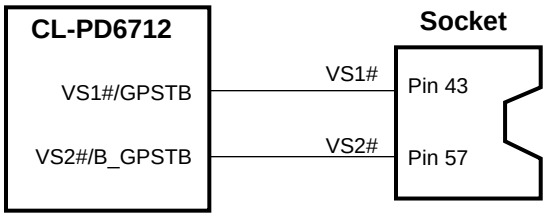
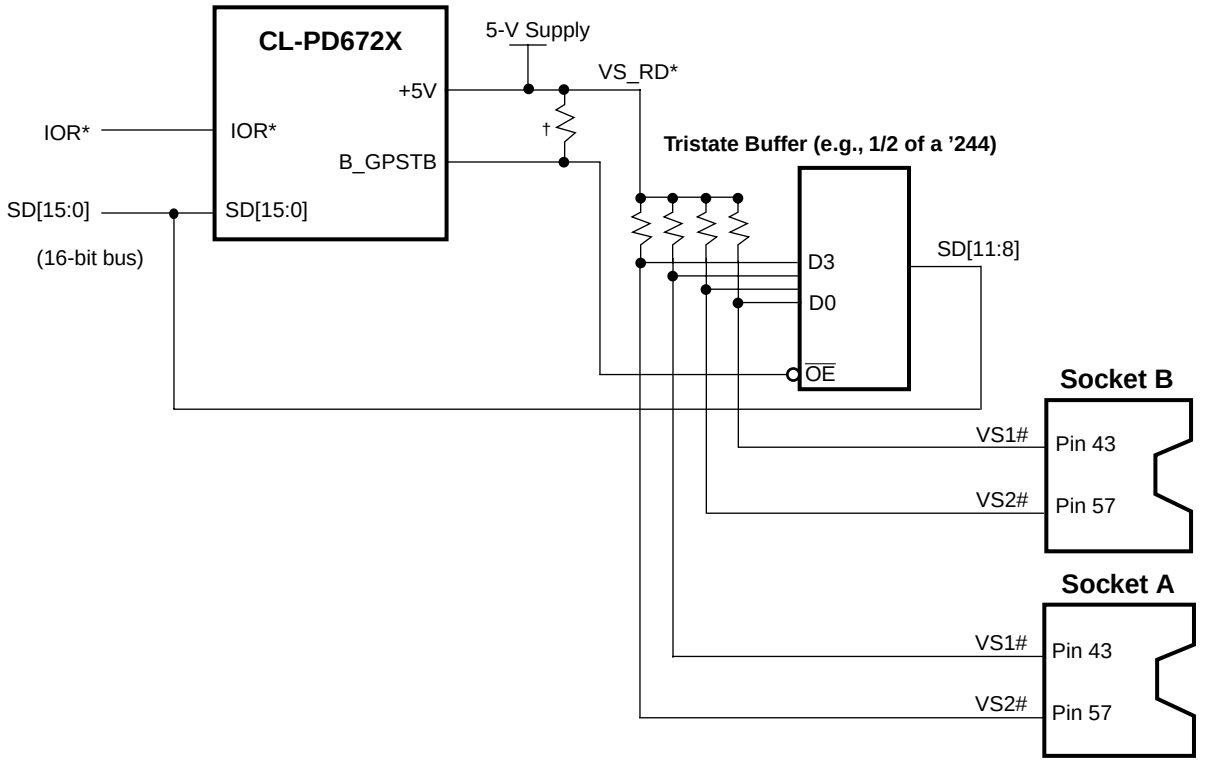


Figure 13-1. VS1# and VS2# Sensing on a CL-PD6712

On the CL-PD672X, the B_GPSTB pin is programmed as a general-purpose read strobe. The VS1# and VS2# pins from the A and B sockets are connected to the external half of a '244 buffer as follows (which allows Socket A VS1 and VS2 to appear as bits 0 and 1, and Socket B VS1 and VS2 to appear as bits 2 and 3):



† Pull-up resistor, or set Extension Control 2 bit 2 to '1' for totem-pole output.

Figure 13-2. VS1# and VS2# Sensing on a CL-PD672X (Socket B Extension Control 2 bit 3 is '1')

14. DMA OPERATION (CL-PD6712 and CL-PD6722)

14.1 DMA Capabilities of the CL-PD6712 and CL-PD6722

The CL-PD6712 and CL-PD6722 include support of a DMA-capable PC Card slave and the movement of DMA data to/from the card with the ISA bus as a DMA master.

Only one socket at a time should be enabled for DMA transfer because the ISA bus DMA handshake signals are shared between both socket interfaces.

DMA transfers to and from the DMA-capable PC Card may be 8- or 16-bit, as indicated by the size of the ISA bus DMA cycle.[1]

14.2 DMA-Type PC Card Cycles

Transfer of DMA data to or from a card is achieved through use of a special DMA-type PC Card interface cycle. This cycle is defined to not conflict with standard PC Card memory or I/O cycles.

A card that is DMA-capable can distinguish PC Card interface cycle types presented by the CL-PD6712 and CL-PD6722 according to the following table:

Table 14-1. Four Card Cycle Types for DMA-Type PC Card Interface

Socket Interface Cycle Type	Function of -WE/-OE	Function of -IORD/-IOWR	Function of -REG
Card Memory Read/Write	Data Transfer Signaling	Always Inactive High	Always Inactive High
Attribute Memory Read/Write	Data Transfer Signaling	Always Inactive High	Always Low
Card I/O Read/Write	Always Inactive High	Data Transfer Signaling	Low = Non-DMA I/O Cycle
Card DMA Data Read/Write	Terminal Count Outputs	Data Transfer Signaling	High = DMA Cycle

NOTE: Bits 7 and 6 of the **Extension Control 1** register must be nonzero for the table to be true; otherwise only standard PC Card cycles will be issued to the card.

The PC Card address is also undefined during the DMA read or write cycle.

Card DMA data read and write cycles transfer DMA data to or from a DMA-capable PC Card. These cycles are distinguished from normal card I/O cycles by the -REG signal being high during the cycle, which is an undefined condition in the PC Card Standard.

[1] Transfer size at socket interface is the same as transfer size on an ISA bus. For 8-bit DMA transfers, connect CL-PD6712 or CL-PD6722 DMA handshake signals to ISA bus DMA channels 0, 1, 2, or 3. For 16-bit transfers, connect CL-PD6712 or CL-PD6722 DMA handshake signals to ISA bus DMA channels 5, 6, or 7.

14.3 ISA Bus DMA Handshake Signal

A DMA request from the card is passed to the ISA bus as long as the socket interface FIFO is empty. IRQ10 is used as the DMA request output to the ISA bus when bit 2 of the **Misc Control 2** register is '1'. When bit 2 of the **Misc Control 2** register is '1', IRQ9 is redefined as the active-low DMA acknowledge input from the ISA bus. This signal must remain active for all DMA transfers through the CL-PD6712 or CL-PD6722.

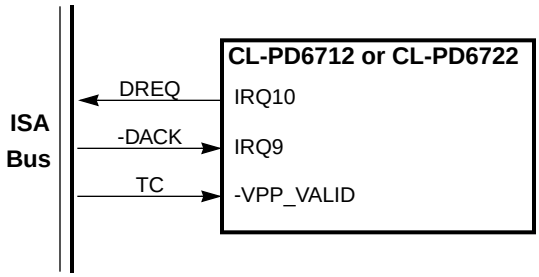


Figure 14-1. DMA Handshake Connections to the ISA Bus to Make the CL-PD6712 or CL-PD6722 DMA-Capable

Terminal counts are passed through to the card from the CL-PD6712 or CL-PD6722 -VPP_VALID pin when bit 6 of the **Misc Control 2** register is '1'. For a DMA write process, the last-cycle terminal count condition is indicated by -OE being active-low during a card DMA data read cycle. For a DMA read process, terminal count is indicated by -WE being active-low during the last card cycle.

14.4 Configuring the CL-PD6712 or CL-PD6722 Registers for a DMA Transfer

Program the registers as follows to configure a CL-PD6712 or CL-PD6722 socket interface for DMA transfer to/from a DMA-capable PC Card:

1. **Select which pin on the PC Card interface will serve as the DMA request input.**
2. **Configure the socket interface as I/O-capable.**
3. **Prevent dual-interpretation of socket interface DMA handshake signals.**
4. **Set the DMA Enable bit.**

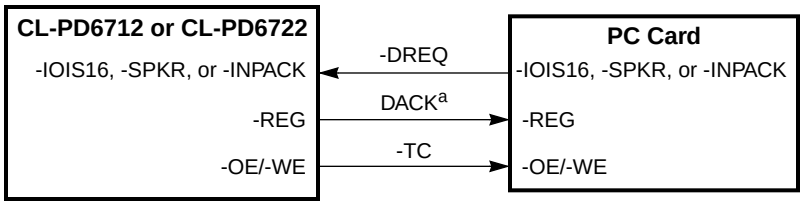
14.4.1 Programming the DMA Request Pin from the Card

The CL-PD6712 and CL-PD6722 allow selection of one of three PC Card interface inputs to be redefined as the DMA request input, and it also allows programming of the active level of the selected input. This is done by setting bits 7 and 6 of the **Extension Control 1** register to the desired values matching those of the DMA-capable PC Card to be used.

Once this selection of DMA request input is complete, the PC Card interface is configured at the signal level for DMA card interfacing.

The following table shows how the CL-PD6712 or CL-PD6722 socket interface signals are redefined when a card is in DMA card interface mode:

Standard I/O Card Interface Signal Name	DMA-Capable Card Interface Signal Usage	When Signal Redefinition for DMA Interface is Effective
-IOIS16	-IOIS16 or may be selected as the active-low DMA request input	**Extension Control 1** register bits 7-6 = '10'
(BVD2/) -SPKR/-LED	-SPKR/-LED or may be selected as the active-low DMA request input	**Extension Control 1** register bits 7-6 = '11'
-INPACK	-INPACK or may be selected as the active-low DMA request input	**Extension Control 1** register bits 7-6 = '01'
-REG	-REG during standard cycles, active-high DACK during DMA read/write cycles	Only during actual card DMA read or write cycle
-OE	-OE during standard cycles, active-low -TC during DMA write cycles	During DMA write cycles (that is, when -REG is high and -IORD is low)
-WE	-WE during standard cycles, active-low -TC during DMA read cycles	During DMA read cycles (that is, when -REG is high and -IOWR is low)



[a] A DMA cycle *is* the DMA acknowledge to the card.

Figure 14-2. Card DMA Request and Acknowledge Handshake with Terminal Count

Notice that DMA acknowledge to the card as -REG high is only active during the actual DMA read or write card cycle. This means there is no mechanism to deassert DACK to the card: the card must understand that receiving the first DMA cycle is its DMA acknowledgment.

14.4.2 Configuring the Socket Interface for I/O

For DMA support, bit 5 of the **Interrupt and General Control** register must be set to '1' to put the card interface in I/O Card Interface mode.

14.4.3 Preventing Dual Interpretation of DMA Handshake Signals

If the WP/-IOIS16 pin is being used as the DMA request line, the following should be considered:

1) Bit 4 of the **Interface Status** register is now the level of the DMA request line from the card.

2) Bit 5 of the socket's two I/O Window Control registers should be set to '0'.

If a socket's BVD2/-SPKR pin is being used as the DMA request line, speaker or LED output from that socket is not available.

If -INPACK is selected as the DMA request input, then bit 7 of the **Misc Control 1** register should be set to '0' to disable use of this signal as input acknowledge control.

No other register bits require special settings to accommodate DMA support on a socket interface.

14.4.4 Turning On DMA System

The DMA System bit (bit 6 of the **Misc Control 2** register) should be programmed to '1' to allow DMA operation and to redefine ISA bus interface pins for DMA support as in Figure 14-1.

14.5 The DMA Transfer Process

As soon as the selected DMA request input from the card becomes active (low) and the FIFO empties, IRQ10 becomes active (high), signifying a DMA request to the system. The system then responds with an active (low) -DACK at IRQ9, which enables the CL-PD6712 or CL-PD6722 to decode any ISA bus DMA transfers that may occur and perform the corresponding transfers at the card. Normal card I/O or memory reads or writes may be interspersed with DMA read and write cycles.

14.6 Terminal Count to Card at Conclusion of Transfer

At the conclusion of each transfer process, systems send active (high) TC (terminal count) pulses to the -VPP_VALID pin during the last DMA cycles to the CL-PD6712 or CL-PD6722.

For a DMA write cycle, TC active is signaled at the socket interface as the -OE pin going low during DMA-type read cycles from the PC Card.

For a DMA read cycle, TC active is signaled as the -WE pin going low during DMA-type write cycles to the PC Card.

15. ELECTRICAL SPECIFICATIONS

15.1 Absolute Maximum Ratings

Description	Absolute Maximum Rating[a]
Ambient temperature under bias	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any pin (with respect to ground)	–0.5 volts to 0.5 volts greater than voltage of +5V pin, respective to ground
Operating power dissipation	500 mW
Suspend power dissipation	10 mW
Power supply voltage	7 volts
Injection current (latch up)	25 mA

[a] Stresses above those listed may cause permanent damage to system components. These are stress ratings only; functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

15.2 DC Specifications

Table 15-1. General DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
C_{IN}	Input Capacitance		10.0	pF	
C_{OUT}	Output Capacitance		10.0	pF	
I_{IL}	Input Leakage	–10.0	10.0	µA	$0 < V_{IN} <$ respective V_{CC} supply pin
I_{PU}	Internal Pull-up Current	–30	–400	µA	

Table 15-2. PC Card Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
$SOCKET\_VCC_{5V}$	Power Supply Voltage	4.5	5.5	V	Normal operation
$SOCKET\_VCC_{3V}$	Power Supply Voltage	3.0	3.6	V	
V_{IH}	Input High Voltage	2.0		V	CORE_VDD = 3.0 V, **Misc Control 2** register, bit 3 is '0'
		2.0		V	CORE_VDD = 4.5 V, **Misc Control 2** register, bit 3 is '1'
V_{IL}	Input Low Voltage		0.8	V	CORE_VDD = 3.6 V, **Misc Control 2** register, bit 3 is '0'
			0.8	V	CORE_VDD = 5.5 V, **Misc Control 2** register, bit 3 is '1'
V_{IHC}	Input High Voltage CMOS	$0.7\ V_{DD}$		V	CORE_VDD = 4.5 V, **Misc Control 2** register, bit 3 is '0'
V_{ILC}	Input Low Voltage CMOS		$0.2\ V_{DD}$	V	CORE_VDD = 5.5 V, **Misc Control 2** register, bit 3 is '0'
V_{OH}	Output High Voltage	2.4		V	At rated I_{OH}, respective SOCKET_VCC = 3.0 V
V_{OHC}	Output High Voltage CMOS	SOCKET_VCC – 0.5		V	At rated I_{OHC}, respective SOCKET_VCC = 3.0 V
V_{OL}	Output Low Voltage		0.5	V	At rated I_{OL}
I_{OH}	Output High Current	–2		mA	Respective SOCKET_VCC = 3.0 V, V_{OH} = 2.4V
I_{OHC}	Output High Current CMOS	–1		mA	Respective SOCKET_VCC = 3.0 V, V_{OHC} = SOCKET_VCC – 0.5 V
I_{OL}	Output Low Current	2		mA	Respective SOCKET_VCC = 3.0 V, V_{OL} = 0.5 V

Table 15-3. ISA Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
ISA_VCC_{5V}	Power Supply Voltage	4.5	5.5	V	Normal operation
ISA_VCC_{3V}	Power Supply Voltage	3.0	3.6	V	Normal operation
V_{IH}[a]	Input High Voltage	2.0		V	CORE_VDD = 3.0 V
V_{IL}[a]	Input Low Voltage		0.8	V	CORE_VDD = 3.6 V
V_{IHC}[a]	Input High Voltage CMOS	0.7 V_{DD}[b]		V	CORE_VDD = 4.5 V
V_{ILC}[a]	Input Low Voltage CMOS		0.2 V_{DD}[b]	V	CORE_VDD = 5.5 V
V_{OH}	Output High Voltage	2.4		V	At rated I_{OH}, ISA_VCC = 3.0 V
V_{OHC}	Output High Voltage CMOS	ISA_VCC – 0.5		V	At rated I_{OHC}, ISA_VCC = 3.0 V
V_{OL}	Output Low Voltage		0.5	V	At rated I_{OL}
I_{OH}	Output Current High, 2-mA-type driver	–2		mA	ISA_VCC = 3.0 V, V_{OH} = 2.4 V
	Output Current High, 12-mA-type driver	–5		mA	
	Output Current High, 16-mA-type driver	–5		mA	
I_{OHC}	Output Current High CMOS, 2-mA-type driver	–1		mA	ISA_VCC = 3.0 V, V_{OHC} = ISA_VCC – 0.5 V
	Output Current High CMOS, 12-mA-type driver	–1		mA	
	Output Current High CMOS, 16-mA-type driver	–1		mA	
I_{OL}	Output Current Low, 2-mA-type driver	2		mA	ISA_VCC = 3.0 V, V_{OL} = 0.5 V
	Output Current Low, 12-mA-type driver	12		mA	
	Output Current Low, 16-mA-type driver	16		mA	

[a] When the CORE_VDD voltage is 3.3 V, input thresholds are TTL compatible; when the CORE_VDD voltage is 5 V, input thresholds are CMOS compatible.

[b] The value of the input threshold level is dependent on the voltage applied to V_{DD} pins of the CL-PD67XX.

Table 15-4. Power Control Interface (+5V Powered) DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
+5V	+5V Supply Voltage	Highest V_{CC} – 0.3	5.5	V	
V_{IH}	Input High Voltage	2.0		V	+5V pin voltage = 4.5 V
V_{IL}	Input Low Voltage		0.8	V	+5V pin voltage = 5.5 V
V_{OH}	Output High Voltage	2.4		V	+5V pin voltage = 4.5 V, I_{OH} = –5 mA
V_{OHC}	Output High Voltage CMOS	+5V voltage – 0.5		V	+5V pin voltage = 4.5 V, I_{OH} = –1 mA
V_{OL}	Output Low Voltage		0.5	V	
I_{OH}	Output Current High, 16-mA-type driver	-5		mA	Respective +5V pin voltage = 4.5 V, V_{OH} = 2.4 V
I_{OHC}	Output Current High CMOS, 16-mA-type driver	–1		mA	Respective +5V pin voltage = 4.5 V, V_{OHC} = +5V pin voltage – 0.5 V
I_{OL}	Output Current Low, 16-mA-type driver	16		mA	Respective +5V pin voltage = 4.5 V, V_{OL} = 0.5 V

Table 15-5. Operating Current Specifications

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$Icc_{tot(1)}$	Power Supply Current, operating	< 6	8	< 20	mA	CORE_VDD = 3.3 V; +5V, SOCKET_VCC, and ISA_VCC = 5.0 V; P_{DISS} = < 85 mW
$Icc_{tot(2)}$	Power Supply Current, Suspend[a]		< 150		µA	CORE_VDD = 3.3 V; +5V, SOCKET_VCC, and ISA_VCC = 5.0 V; P_{DISS} = < 2 mW
$Icc_{tot(3)}$	Power Supply Current, Super Suspend, No Clocks[a]		< 20		µA	CORE_VDD = 3.3 V; +5V, SOCKET_VCC, and ISA_VCC = 5.0 V; P_{DISS} = < 1 mW

[a] No cards in sockets; or for CL-PD6712 or CL-PD6722, bit 5 of the **DMA Control** register is a '1'.

15.3 AC Timing Specifications

This section includes system timing requirements for the CL-PD67XX. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0°C to 70°C, and V_{CC} varying from 3.0 to 3.6 V or 4.5 to 5.5 V DC. The AT bus speed is 10 MHz unless otherwise noted. Note that an asterisk (*) denotes an active-low signal for the ISA bus interface, and a dash (-) denotes an active-low signal for the PC Card socket interface.

Additionally, the following statements are true for all timing information:

- All timings assume a load of 50 pF.
- TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

Table 15-6. List of AC Timing Specifications

15.3.1 ISA Bus Timing

Table 15-7. ISA Bus Timing

Symbol	Parameter	MIN	MAX	Unit
t_1	MEMCS16* active delay from LA[23:17] valid		40	ns
t_{1a}	LA[23:17] setup to ALE inactive	30		ns
t_{1b}	LA[23:17] hold from ALE inactive	5		ns
t_2	IOCS16* active delay from SA[15:0][1]		40	ns
t_{2a}	IOCS16* inactive delay from SA[15:0][1]		40	ns
t_3	SA[16:0], SBHE* setup to any Command active[1, 2] LA[23:17] latching by ALE to any Command active	30 90		ns ns
t_4	Any Command active to IOCHRDY inactive (low)[3]		40	ns
t_{4a}	IOCHRDY three-state from Command inactive[4]	5	30	
t_5	MEMCS16* inactive delay from unlatched LA[23:17]		40	ns
t_{6a}	IOW* or IOR* pulse width[1]	140		ns
t_{6b}	MEMW* or MEMR* pulse width[1]	180		ns
t_7	Any Command inactive to next Command active	100		ns
t_8	Address or SBHE* hold from any Command inactive	0		ns
t_9	Data valid from MEMW* active[5] Data valid from IOW* active		40 40	ns ns
t_{10}	Data hold from MEMW* inactive Data hold from IOW* inactive	5 5		ns ns
t_{11}	Data delay from IOR* active, for internal registers	0	130	ns
t_{12}	Data delay from IOCHRDY active		15	ns
t_{13}	Data hold from IOR* or MEMR* inactive	0	30	ns
t_{14}	AEN inactive setup to valid IOR* or IOW* active	40		ns
t_{15}	AEN hold from IOR* or IOW* inactive	5		ns
t_{16}	REFRESH* inactive setup to valid MEMR* or MEMW* active	40		ns
t_{17}	REFRESH* inactive hold from MEMR* or MEMW* active	0		ns
t_{18}	MEMCS16* active delay from SA[16:12] valid		40	ns
t_{19}	*ZWS delay from MEMW* active		30	ns
t_{20}	*ZWS hold from MEMW* inactive		15	ns

1 AEN must be inactive for t_2, t_3, and t_6 timing specifications to be applicable.
2 Command is defined as IOR*, IOW*, MEMR*, or MEMW*.
3 Except for valid card memory writes, which are zero wait state when internal write FIFO is not full.
4 If card is removed during a card access cycle, IOCHRDY is three-stated without waiting for end of Command.
5 Based on 25-MHz internal clock, produced either by an internal synthesizer and 14.318-MHz signal applied to CLK pin, or by supplying 25 MHz directly to CLK pin and bypassing the internal synthesizer.

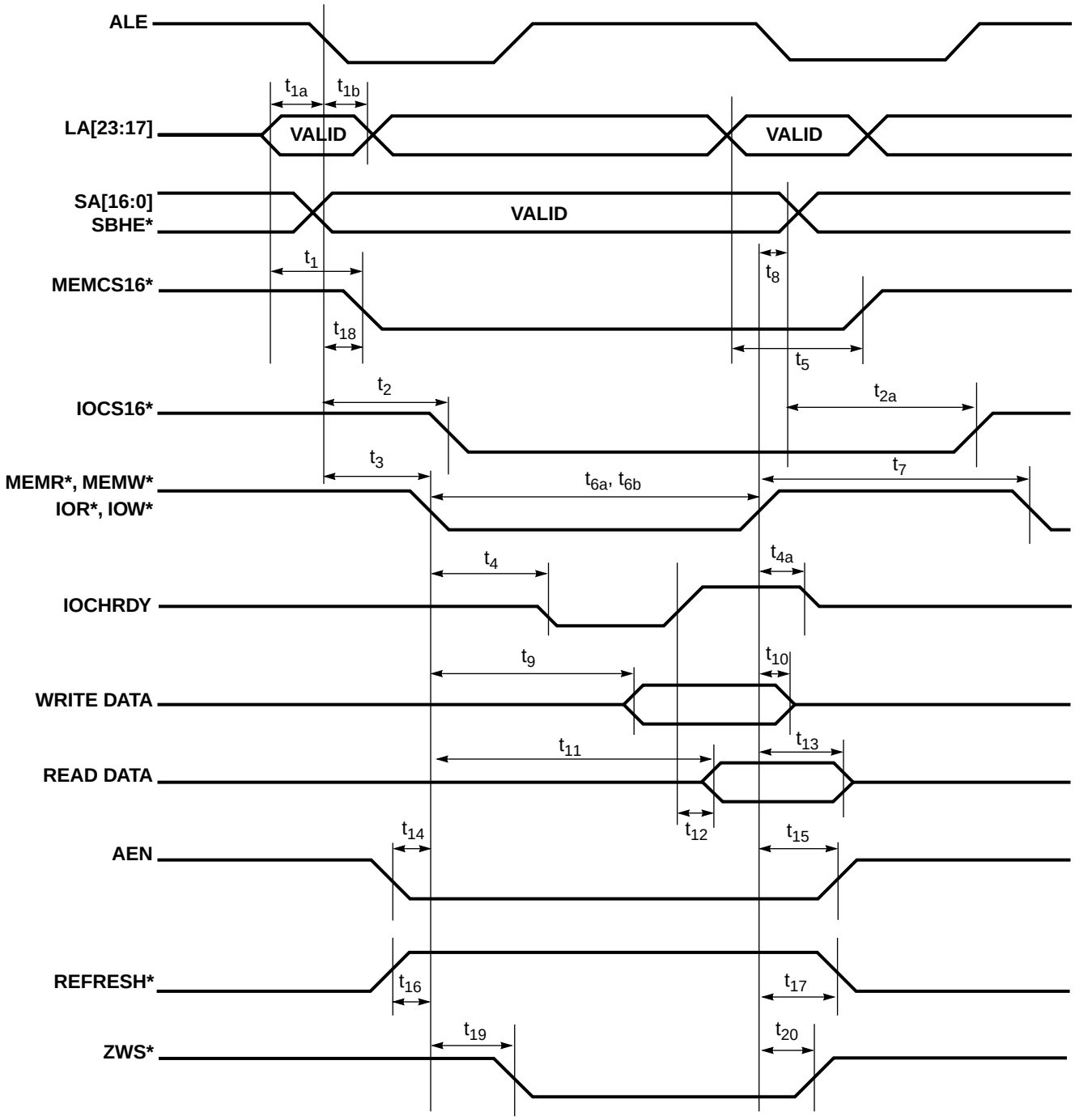


Figure 15-1. Bus Timing — ISA Bus

15.3.2 Reset Timing

Table 15-8. Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	PWRGOOD generated reset pulse width	500		ns
t_2	Clock active before end of reset[1]	500		ns
t_3	End of PWRGOOD generated reset to first Command	500		ns

1 Clock input must be active for a minimum of 500 ns before PWRGOOD goes active to allow sufficient internal clocks to initialize internal circuitry.

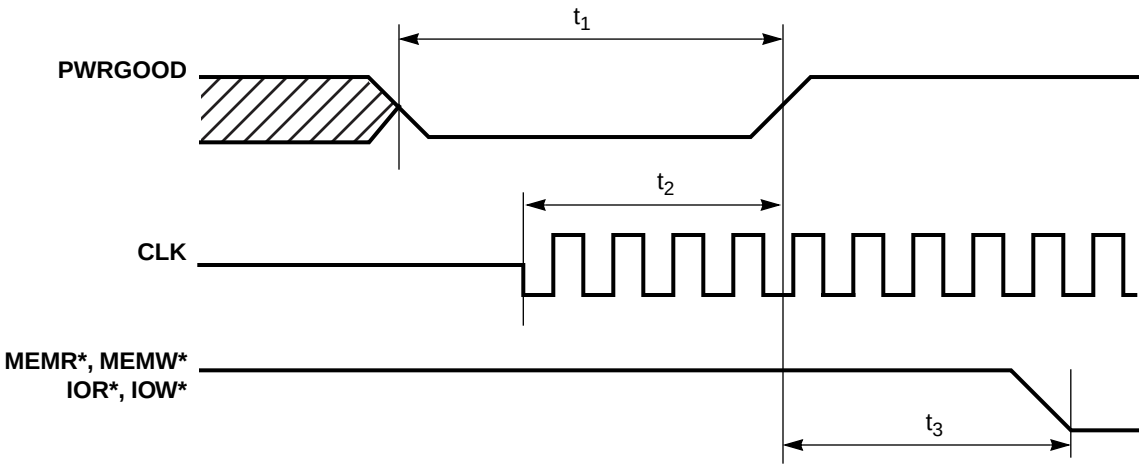
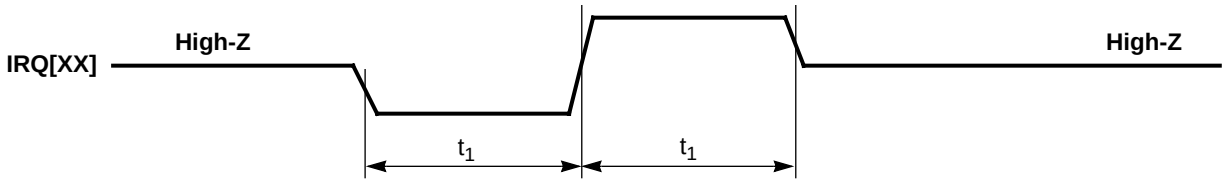


Figure 15-2. Reset Timing

15.3.3 System Interrupt Timing

Table 15-9. Pulse Mode Interrupt Timing

Symbol	Parameter	MIN	MAX
t_1	IRQ[XX] low or high	2 CLK – 10 ns	2 CLK + 10 ns



High-Z = high impedance

NOTE: Each time indicated is 2 clock periods of the CLK input to the CL-PD67XX, independent of setting of the Bypass Frequency Synthesizer bit.

Figure 15-3. Pulse Mode Interrupt Timing

15.3.4 General-Purpose Strobe Timing

Table 15-10. General-Purpose Strobe Timing

Symbol	Parameter	MIN	MAX	Units
t_1	GPSTB delay after IOR* or IOW* active		40	ns
t_2	GPSTB delay after IOR* or IOW* inactive		40	ns

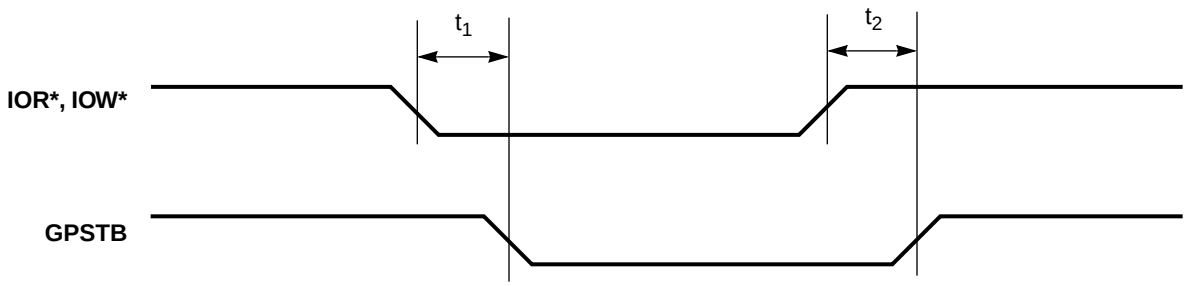


Figure 15-4. General-Purpose Strobe Timing

15.3.5 Input Clock Specification

Table 15-11. Input Clock Specification

Symbol	Parameter	MIN	MAX	Units	Conditions
t_1	CLK pin input rise time	1	7	ns	
t_2	CLK pin input fall time	1	7	ns	
t_3	CLK input low period	0.4 T_{CLKP}	0.6 T_{CLKP}	ns	
t_4	CLK input high period	0.4 T_{CLKP}	0.6 T_{CLKP}	ns	
V_{center}	Center voltage at which period specified	0.5 V_{DD}	0.5 V_{DD}	V	
T_{CLKP}	Input clock period, internal clock	69.84 – 0.1%	69.84 + 0.1%	ns	Normal synthesizer operation. Misc Control 2 register, bit 0 = '0'. CLK pin at 14.318 MHz.
T_{CLKP}	Input clock period, external clock	40 – 0.1%	40 + 0.1%	ns	Synthesizer bypassed. Misc Control 2 register, bit 0 = '1'. CLK pin at 25 MHz.
V_{IHmin}	CLK input high voltage	2.0		V	CORE_VDD = 3.0 V
V_{ILmax}	CLK input low voltage		0.8	V	CORE_VDD = 3.6 V
V_{IHCmin}	CLK input high voltage	0.7 V_{DD}		V	CORE_VDD = 4.5 V
V_{ILCmax}	CLK input low voltage		0.2 V_{DD}	V	CORE_VDD = 5.5 V

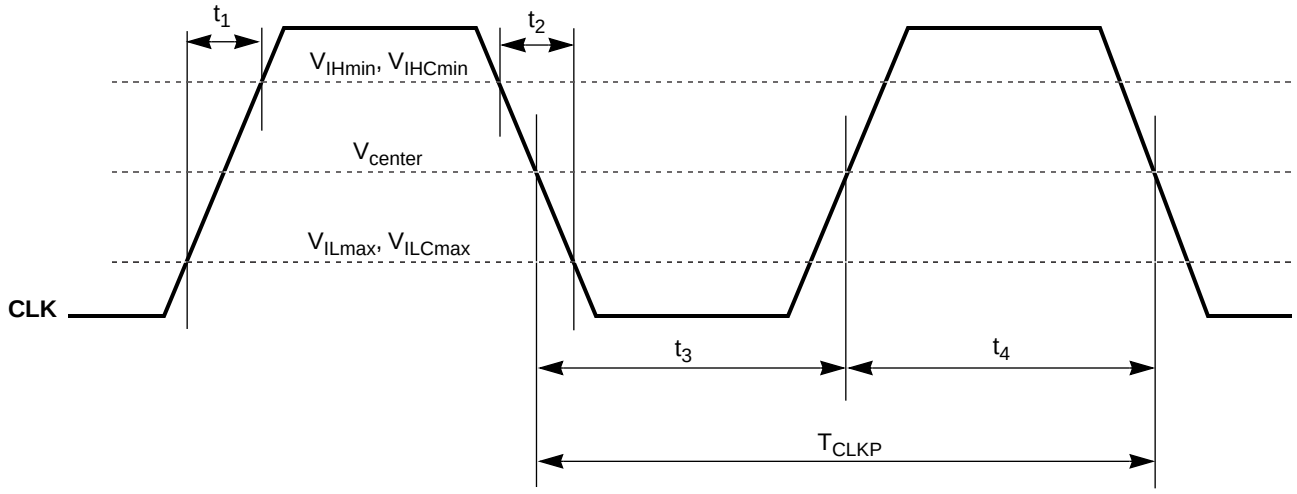


Figure 15-5. Input Clock Specification

15.3.6 PC Card Bus Timing Calculations

Calculations for minimum PC Card cycle Setup, Command, and Recovery timings are made by first calculating factors derived from the applicable timer set's timing registers and then by applying the factor to an equation relating it to the internal clock period.

The PC Card cycle timing factors, in terms of the number of internal clocks, are calculated as follows:

$$S = (N_{pres} \times N_{val}) + 1 \quad \textbf{Equation 15-1}$$

$$C = (N_{pres} \times N_{val}) + 1 \quad \textbf{Equation 15-2}$$

$$R = (N_{pres} \times N_{val}) + 1 \quad \textbf{Equation 15-3}$$

N_{pres} and N_{val} are the specific selected prescaler and multiplier value from the timer set's Setup, Command, and Recovery Timing registers (see Chapter 10 for description of these registers).

From this, a PC Card cycle's Setup, Command, and Recovery time for the selected timer set are calculated as follows:

$$\text{Setup time} = (S \times Tcp) \pm 10 \text{ ns} \quad \textbf{Equation 15-4}$$

$$\text{Command time} = (C \times Tcp) \pm 10 \text{ ns} \quad \textbf{Equation 15-5}$$

$$\text{Recovery time} = (R \times Tcp) \pm 10 \text{ ns} \quad \textbf{Equation 15-6}$$

When the internal synthesizer is used, the calculation of the internal clock period *Tcp* is:

$$Tcp = T_{CLKP} \times 4/7 \quad \textbf{Equation 15-7}$$

where T_{CLKP} is the period of the clock supplied to the CLK input pin. An input frequency of 14.318 MHz at the CLK input pin results in an internal clock period of *Tcp* = 40 ns.

When the internal synthesizer is bypassed, $Tcp = T_{CLKP}$. An input frequency of 25 MHz in this circumstance would also result in an internal clock period of *Tcp* = 40 ns.

The timing diagrams that follow were derived for a CL-PD67XX using the internal synthesizer and a 14.318-MHz CLK pin input. The internal clock frequency of the CL-PD67XX is 7/4 of this incoming signal (*Tcp* = 40 ns). The examples are for the default values of the Timing registers for Timer Set 0, as follows:

Timing Register Name (Timer Set 0)	Index	Value (Default)	Resultant N_{pres}	Resultant N_{val}
Setup Timing 0	3Ah	01h	1	1
Command Timing 0	3Bh	06h	1	6
Recovery Timing 0	3Ch	03h	1	3

Thus the minimum times for the default values are as follows:

$$\text{Default minimum Setup time} = (S \times Tcp) - 10 \text{ ns} = \{2 \times 40 \text{ ns}\} - 10 \text{ ns} = 70 \text{ ns} \quad \textbf{Equation 15-8}$$

$$\text{Default minimum Command time} = (C \times Tcp) - 10 \text{ ns} = \{7 \times 40 \text{ ns}\} - 10 \text{ ns} = 270 \text{ ns} \quad \textbf{Equation 15-9}$$

$$\text{Default minimum Recovery time} = (R \times Tcp) - 10 \text{ ns} = \{4 \times 40 \text{ ns}\} - 10 \text{ ns} = 150 \text{ ns} \quad \textbf{Equation 15-10}$$

15.3.7 PC Card Socket Timing

Table 15-12. Memory Read/Write Timing (Word Access)

Symbol	Parameter	MIN	MAX	Units
t_1	-CE[2:1], -REG, Address, and Write Data setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 10		ns
t_4	-WAIT active from Command active[4]		(C – 2)Tcp – 10	ns
t_5	Command hold from -WAIT inactive	(2 Tcp) + 10		ns
t_6	Data valid from -WAIT inactive		Tcp + 10	ns
t_7	Data setup before -OE inactive	(2 Tcp) + 10		ns
t_8	Data hold after -OE inactive	0		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

4 For typical active timing programmed at 280 ns, maximum -WAIT timing is 190 ns after Command active.

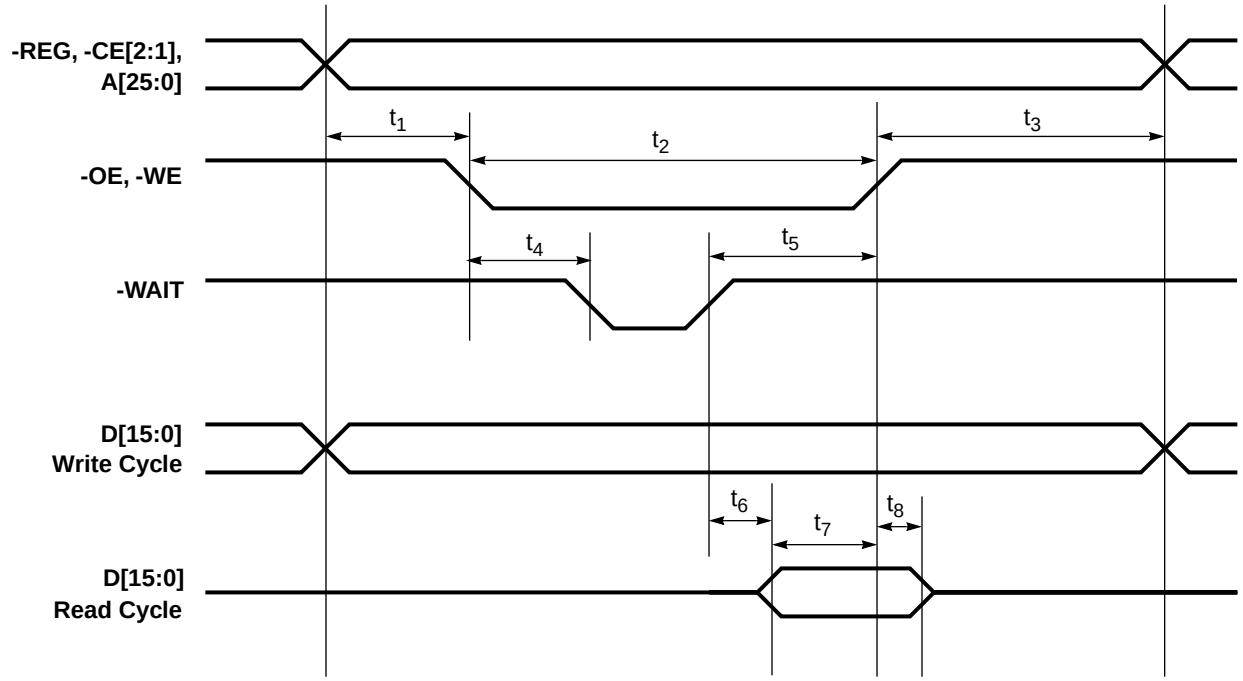


Figure 15-6. Memory Read/Write Timing

Table 15-13. Word I/O Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 10		ns
t_4	-WAIT active from Command active[4]		(C – 2)Tcp – 10	ns
t_5	Command hold from -WAIT inactive	(2 Tcp) + 10		ns
t_{ref}	Card -IOIS16 delay from valid Address (PC Card specification)		35	ns
t_6	-IOIS16 setup time before Command end	(3 Tcp) + 10		ns
t_7	-CE2 delay from -IOIS16 active[5]	Tcp – 10		ns
t_6	Data valid from -WAIT inactive		Tcp + 10	ns
t_9	Data setup before -IORD inactive	(2 Tcp) + 10		ns
t_{10}	Data hold after -IORD inactive	0		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

4 For typical active timing programmed at 280 ns, maximum -WAIT timing is 190 ns after Command active.

5 -IOIS16 must go low within 3Tcp + 10 ns of the cycle beginning or -IOIS16 will be ignored and -CE will not be activated.

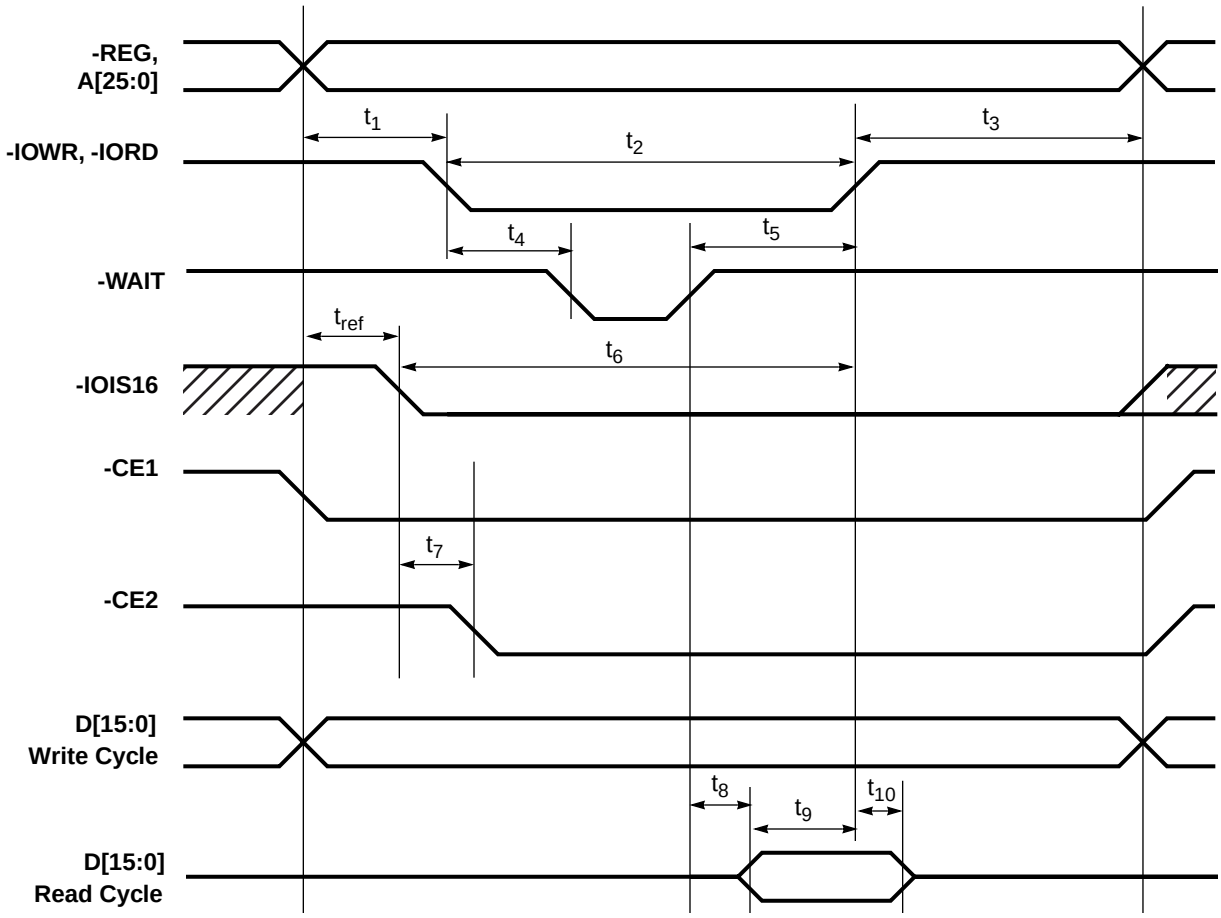


Figure 15-7. Word I/O Read/Write Timing

Table 15-14. PC Card Read/Write Timing when System Is 8-Bit

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 10		ns
t_4	Data setup before Command inactive	(2 Tcp) + 10		ns
t_5	Data hold after command inactive	0		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

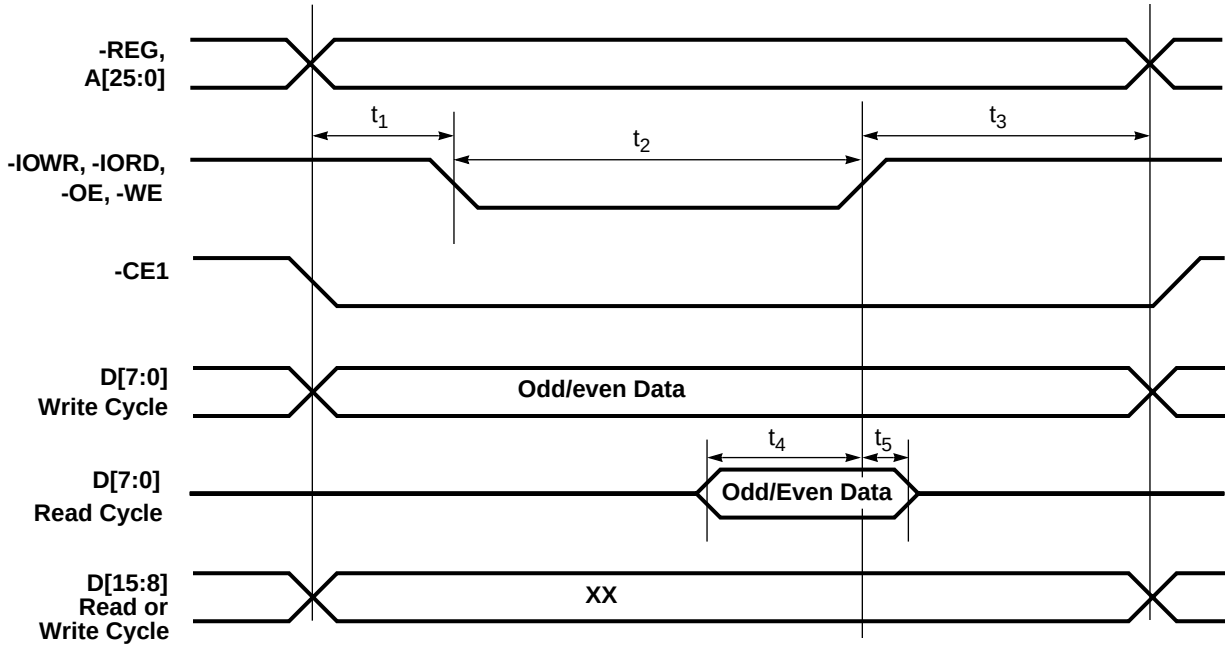


Figure 15-8. PC Card Read/Write Timing when System Is 8-Bit ($\overline{SBHE}$ Tied High)

Table 15-15. Normal Byte Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 10		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

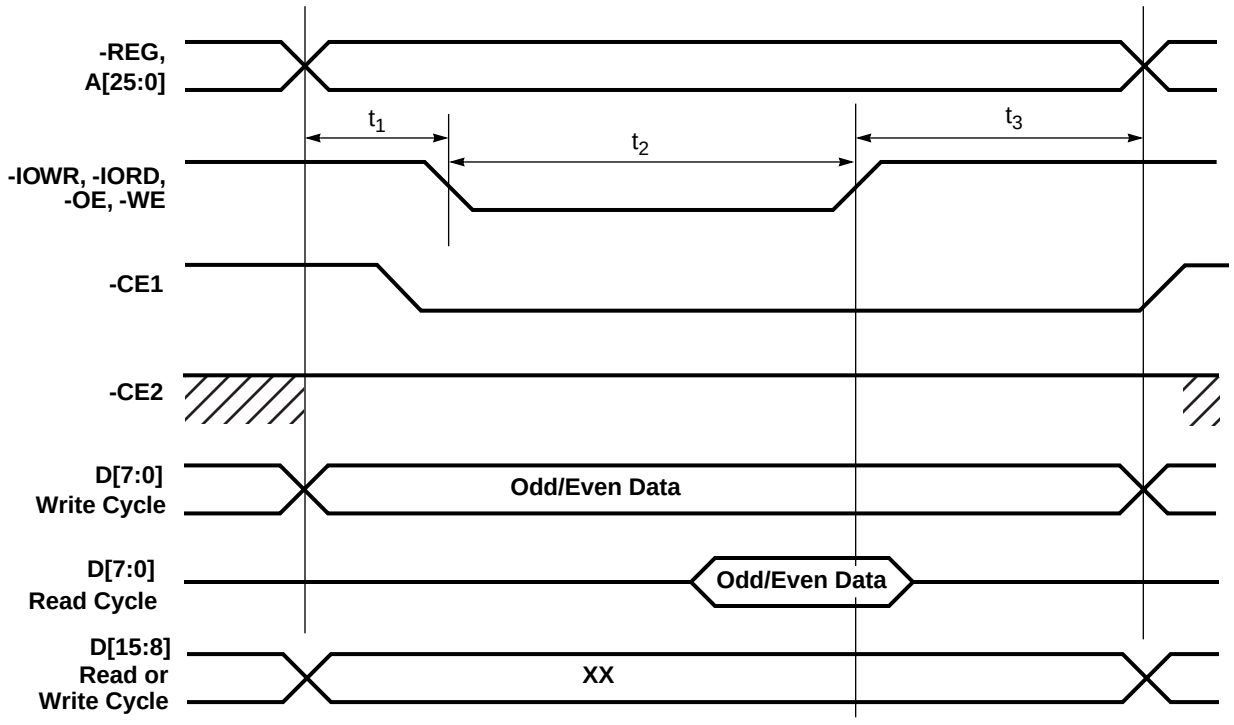


Figure 15-9. Normal Byte Read/Write Timing (that is., all other byte accesses, including odd I/O cycles where -IOIS16 is low)

Table 15-16. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address change to -IOIS16 inactive[4]		(3Tcp) + 10	ns
t_2	-IOIS16 inactive to -CE2 inactive		20	ns
t_3	-IOIS16 inactive to -CE1 active		20	ns
t_4	Address setup to Command active[1]	(S × Tcp) – 10		ns
t_5	Command pulse width[2]	(C × Tcp) – 10		ns
t_6	Address hold from Command inactive[3]	(R × Tcp) – 10		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

4 -IOIS16 level from card should be valid before -IOWR/-IORD goes active. For a typical setup time of 70 ns, a PC Card meeting the PCMCIA specification for -IOIS16 from A[25:0] change will meet this condition.

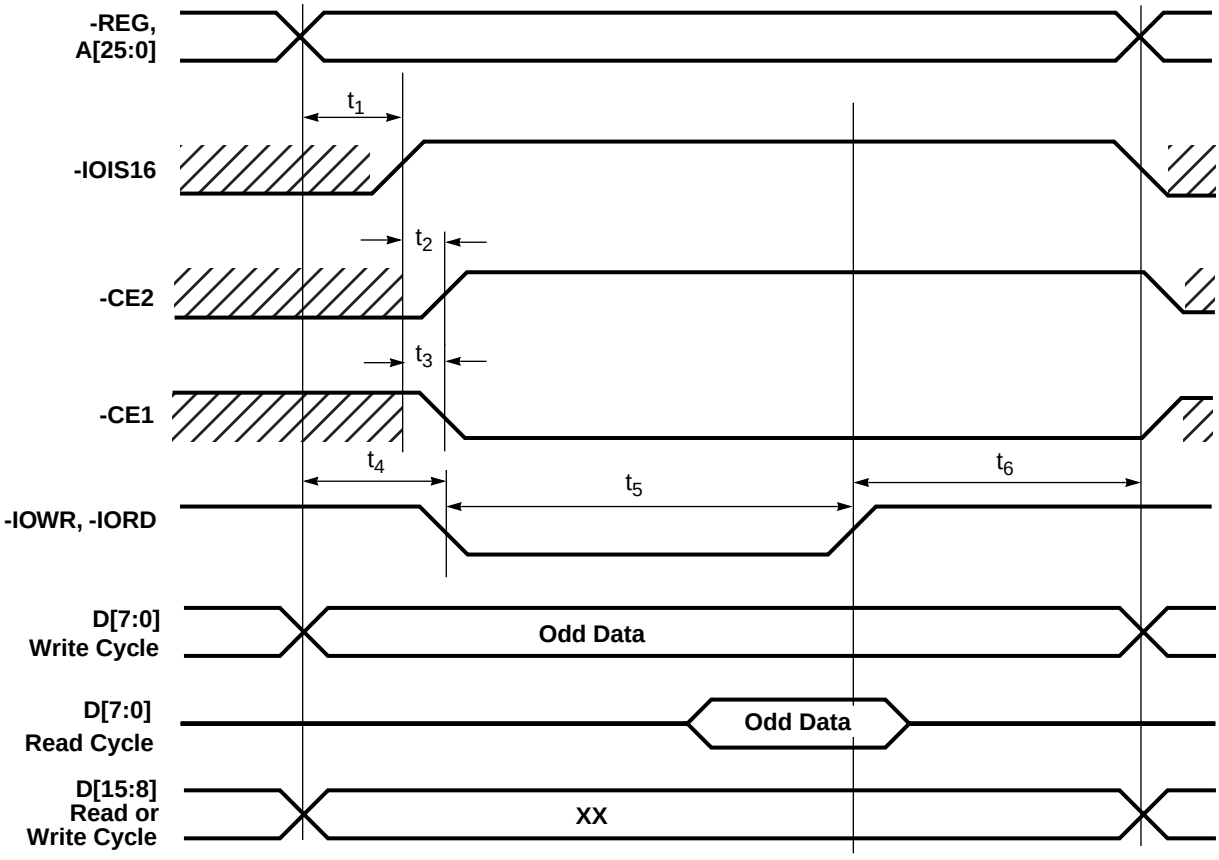


Figure 15-10. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Table 15-17. DMA Read Cycle Timing

Symbol	Parameter	MIN	MAX	Units
t_1	DRQ (IRQ10) and DACK* (IRQ9) active to DMA cycle begin	40		ns
t_2	-CE[2:1], -REG, -IORD, -OE, and Write Data setup to -IOWR active[1]	(S × Tcp) – 10		ns
t_3	Command: -IOWR pulse width[2]	(C × Tcp) – 10		ns
t_4	Recovery: -IOWR inactive to end of cycle[3]	(R × Tcp) – 10		ns
t_5	-WAIT active from -IOWR active		(C – 2)Tcp – 10	ns
t_6	-WAIT inactive to -IOWR inactive	2 Tcp		ns
t_7	System TC (-VPP_VALID high) to -IOWR	–40		ns
t_8	-IOWR to begin of card TC (-WE)[4]	25	50	ns
t_9	End of card TC (-WE) to -IOWR inactive[4]	25	50	ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

[4] Based on an internal clock period of 40 ns (25 MHz).

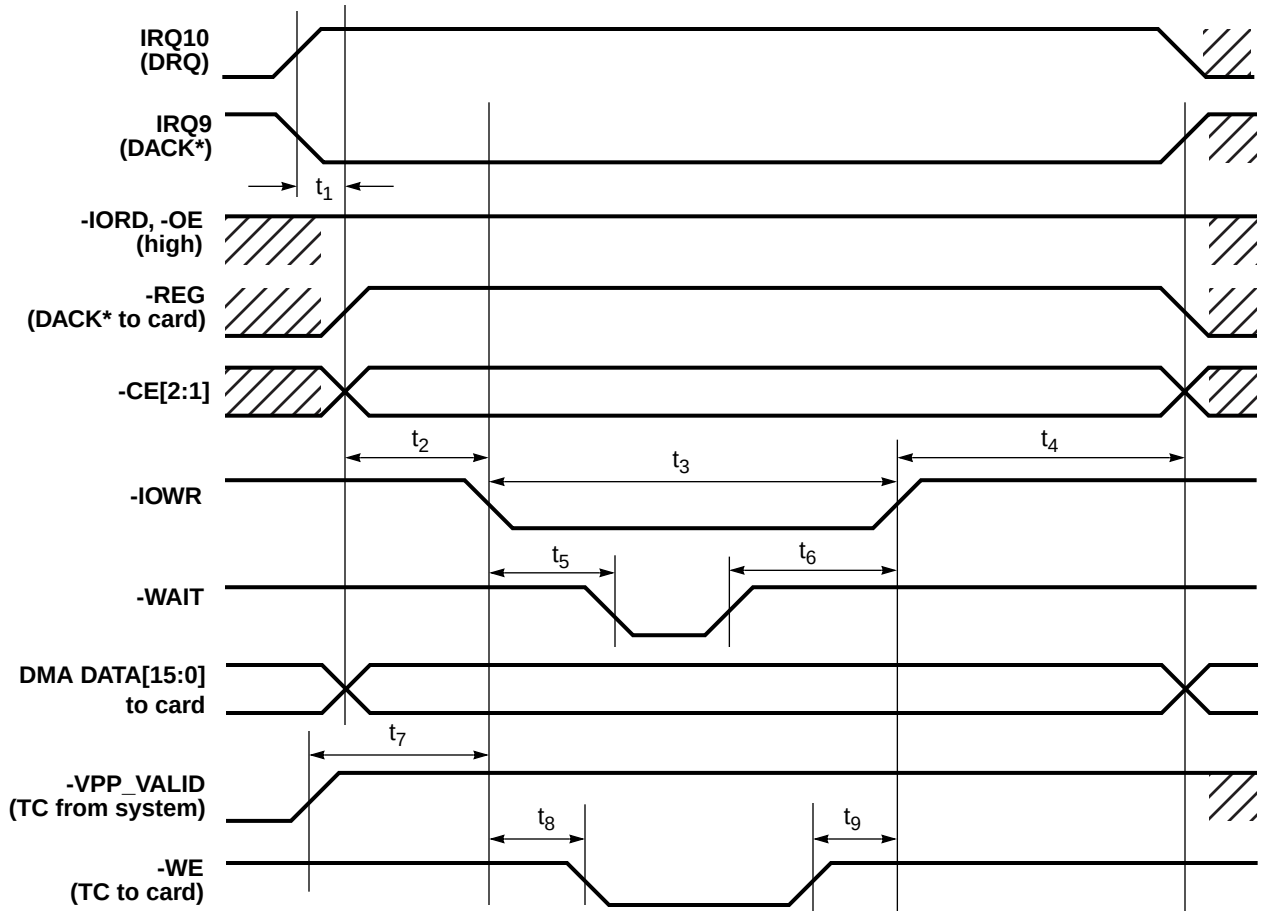


Figure 15-11. DMA Read Cycle Timing

Table 15-18. DMA Write Cycle Timing

Symbol	Parameter	MIN	MAX	Units
t_1	DRQ (IRQ10) and DACK* (IRQ9) active to DMA cycle begin	40		ns
t_2	-CE[2:1], -REG, -IOWR, -WE, and Write Data setup to -IORD active[1]	(S × Tcp) – 10		ns
t_3	Command: -IORD pulse width[2]	(C × Tcp) – 10		ns
t_4	Recovery: -IORD inactive to end of cycle[3]	(R × Tcp) – 10		ns
t_5	-WAIT active from -IORD active		(C – 2)Tcp – 10	ns
t_6	-WAIT inactive to -IORD inactive	2 Tcp		ns
t_7	System TC (-VPP_VALID high) to -IORD	–40		ns
t_8	-IORD to begin of card TC (-OE)[4]	25	50	ns
t_9	End of card TC (-OE) to -IORD inactive[4]	25	50	ns
t_{10}	Data valid from -WAIT inactive	Tcp + 10		ns
t_{11}	Data setup before -OE inactive	(2 Tcp) +10		ns
t_{12}	Data hold after -OE inactive	0		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 98.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 06h, the Command time would be 270 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 98.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 03h, the hold (Recovery) time would be 150 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 98.

4 Based on an internal clock period of 40 ns (25 MHz).

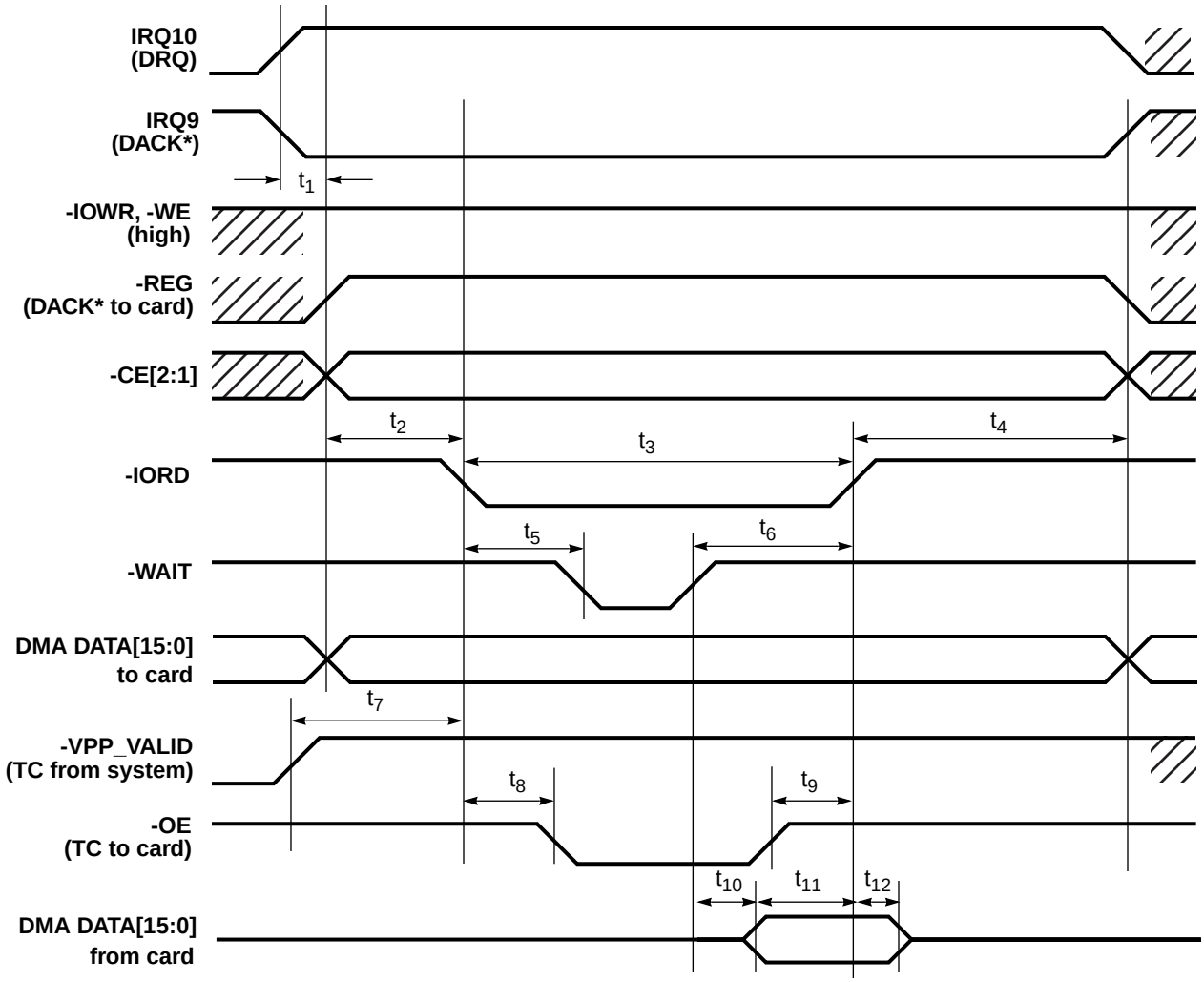
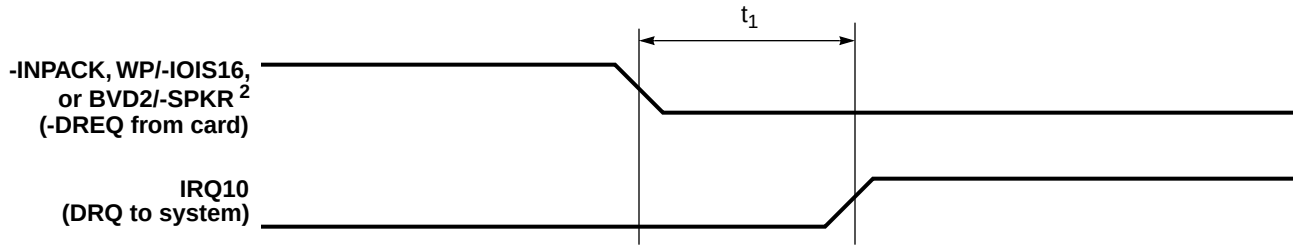


Figure 15-12. DMA Write Cycle Timing

Table 15-19. DMA Request Timing

Symbol	Parameter	MIN	MAX	Units
t_1	DMA request from socket interface to system[1]	40		ns

[1] After FIFO empty, DMA requests held off from being presented to the system until all write data to a card has been emptied from the socket interface FIFO.

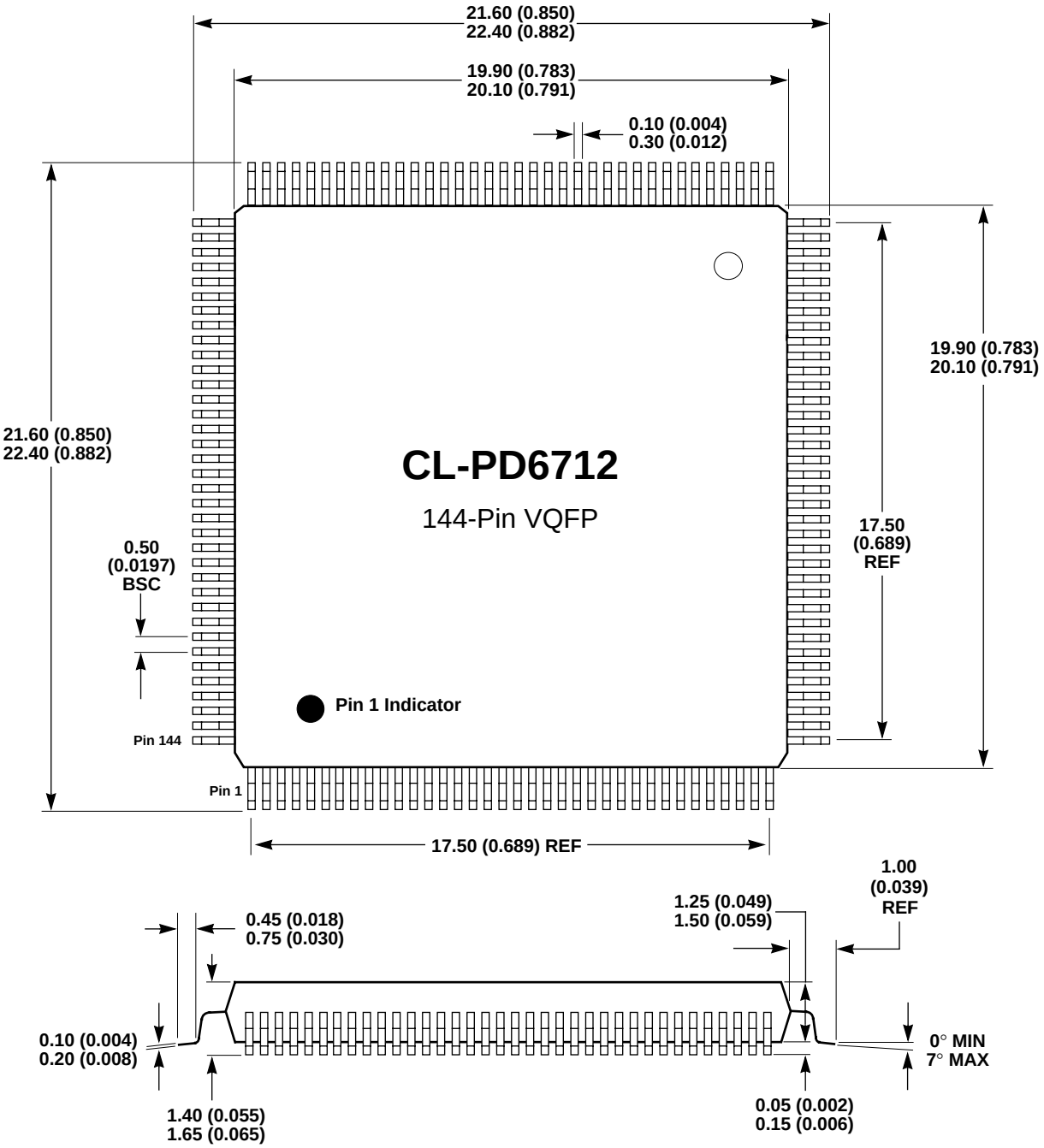


[2] **DMA Control** register bits 7 and 6 define which of these three signals serve as the active-low DMA request from the card.

Figure 15-13. DMA Request Timing

16. PACKAGE SPECIFICATIONS

16.1 144-Pin VQFP Package

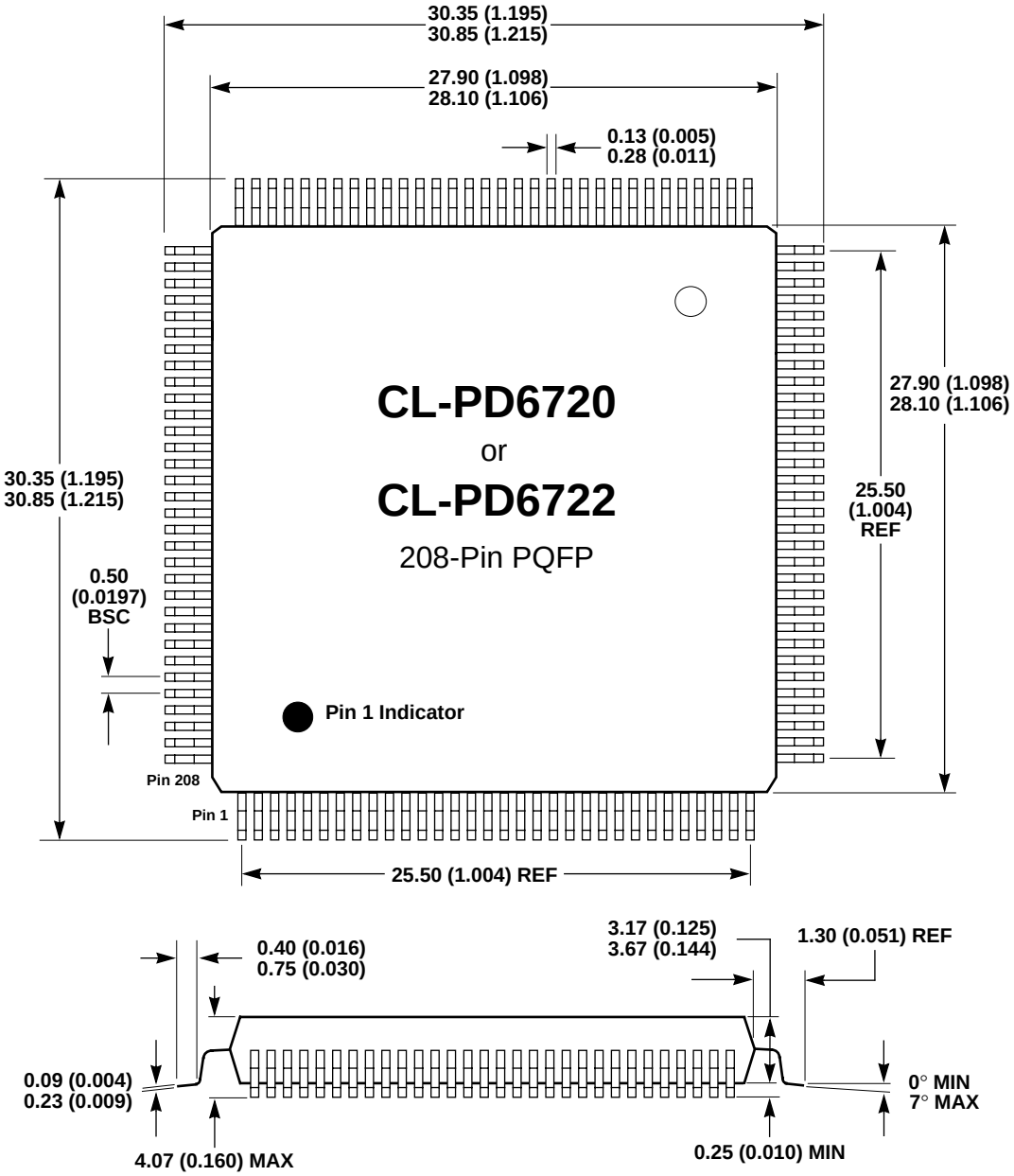


NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.

2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

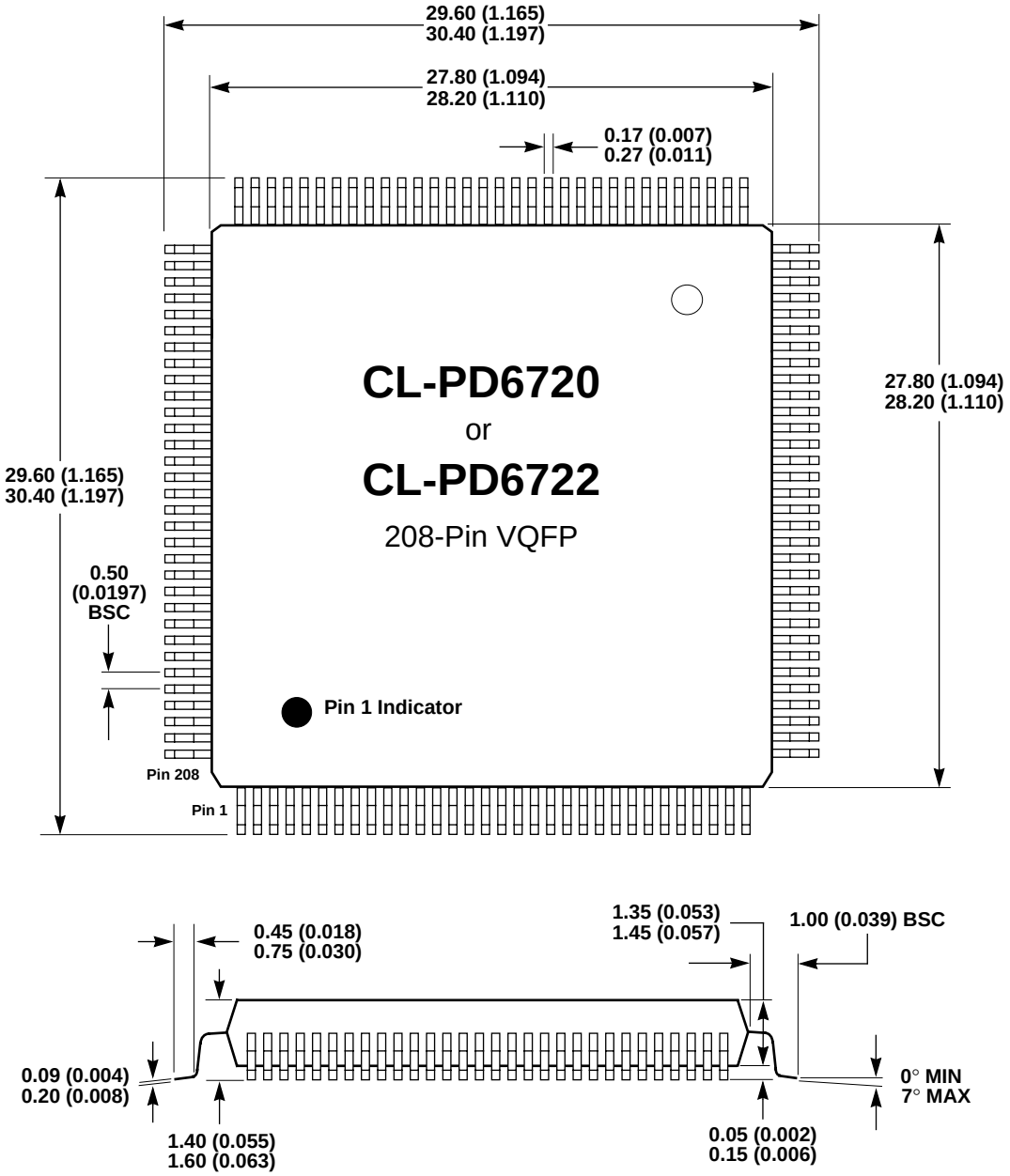
16.2 208-Pin PQFP Package



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is inches.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

16.3 208-Pin VQFP Package

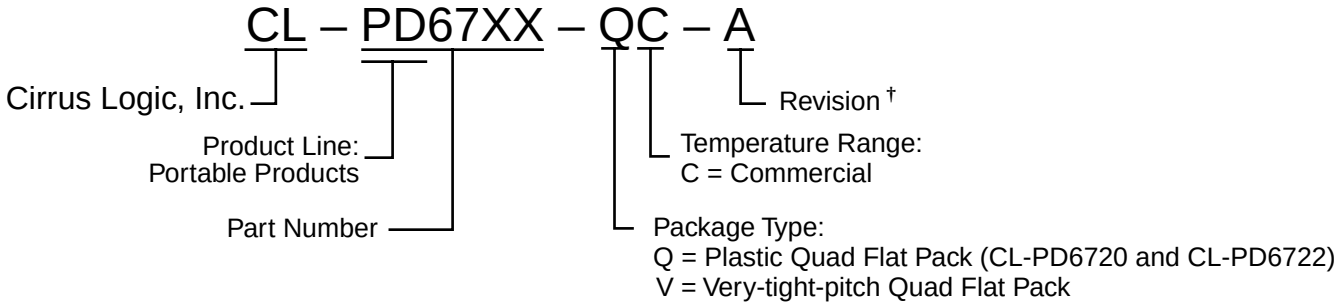


NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is inches.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

17. ORDERING INFORMATION EXAMPLE

The order number for the part is:



† Contact Cirrus Logic for up-to-date information on revisions.

Appendix A

Using the Cirrus Logic BBS and FTP Server

Using the Cirrus Logic BBS

Cirrus Logic maintains a BBS (bulletin board system) 24 hours a day for customers to obtain up-to-date files and information. For the CL-PD67XX, the BBS gives access to utilities, schematics, and software upgrades.

Cirrus Logic strictly controls access to this BBS. All downloadable files are checked by Cirrus Logic and customers cannot upload files to any publicly downloadable area.

Follow the steps that follow to download files. If you would like access to more restricted files, or would like to exchange files with Cirrus Logic personnel on a regular basis, contact your Cirrus Logic representative to obtain expanded access privileges.

1. **Set your communication parameters as follows:**
   - 8 data bits
   - No parity
   - 1 stop bit
   - Baud rate up to 14,400 bps
2. **Dial the Cirrus Logic BBS at (510) 440-9080.**
3. **When connected, do one of the following:**
   - Enter your name and password. First-time users can establish an account by entering a name and password and completing the questionnaire.
   - Or, follow the instructions to log on as a 'guest'.
4. **Select [J] Join Product Area.**
5. **Select [19] 67XX.**
6. **Select [F] File Menu.**
7. **You can now choose among the options.**

   Many BBS files are compressed in a 'zipped' file format (using PKZIP.EXE version 2.04G). These files have the suffix .ZIP appended to their names. They need to be uncompressed after downloading using PKUNZIP.EXE. If you do not have this 'unzip' utility, you can download it in a self-extracting form from the Cirrus Logic BBS — from any area, download the file called PKZ204G.EXE.

Using the FTP Server

In addition to the BBS, Cirrus Logic maintains an anonymous FTP site on the internet. The address is `ftp.cirrus.com`. Using any password, you can log on as anonymous or FTP.

You can also access this site using a World-Wide Web browser by linking from the Cirrus Logic home page at the address `http://www.cirrus.com/`.

NOTE: The FTP server is limited to released software drivers. BIOS, schematics, and beta software is available only on the BBS and is restricted to licensed OEMs.

When you log into the FTP site, you will be in the FTP directory. Change directories to `/pub/support`. This the main directory of the FTP site.

In the `support` directory, a document named `ftp_contents.doc` shows the FTP file names and their contents. Like the BBS, the FTP site is arranged by chip set. The `support` directory provides access to the desktop, laptop, modem, PCMCIA, and SIO areas. Within these directories are the chip-set subdirectories. Within these subdirectories are software files.

Appendix B

Register Summary Tables

B.1 Operation Registers

Register Name: **Index** *Register Per:* chip
Index: **n/a** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Device Index	Socket Index	Register Index					
RW:0	RW:0	RW:000000					

Register Name: **Data** *Register Per:* chip
Index: **n/a** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Data							

B.2 Chip Control Registers

Register Name: **Chip Revision** *Register Per:* chip
Index: **00h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Interface ID		*0*	*0*	Revision			
R:10		R:0	R:0	R:0010[a]			

[a] Value for the current stepping only.

Register Name: **Interface Status** *Register Per:* socket
Index: **01h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
-VPP_VALID		*RDY*	*WP*	*-CD2*	*-CD1*	*BVD2*	*BVD1*
V_{PP} Valid	Card Power On	Ready/Busy*	Write Protect	Card Detect		Battery Voltage Detect	
R[a]	R:0	R[b]	R[c]	R[d]		R[e]	

[a] Bit 7 is the inversion of the value of the -VPP_VALID pin (see page 15).
[b] Bit 5 is the value of the RDY/-IREQ pin (see page 17).
[c] Bit 4 is the value of the WP/-IOIS16 pin (see page 17).
[d] Bits 3:2 are the inversion of the values of the -CD1 and -CD2 pins (see page 18).
[e] Bits 1:0 are the values of the BVD1/-STSCHG and BVD2/-SPKR pins (see page 18).

Register Name: **Power Control** — *Register Per:* socket
Index: **02h** — *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Card Enable	*Compatibility Bit*	Auto-Power	V_{CC} Power	*Compatibility Bits*		V_{PP}1 Power	
RW:0	RW:0	RW:0	RW:0	RW:00		RW:00	

Register Name: **Interrupt and General Control** — *Register Per:* socket
Index: **03h** — *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Ring Indicate Enable	Card Reset*	Card Is I/O	Enable Management Interrupts	Card IRQ Select			
RW:0	RW:0	RW:0	RW:0	RW:0000			

Register Name: **Card Status Change** — *Register Per:* socket
Index: **04h** — *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
0	*0*	*0*	*0*	Card Detect Change	Ready Change	Battery Warning Change	Battery Dead Or Status Change
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

Register Name: **Management Interrupt Configuration** — *Register Per:* socket
Index: **05h** — *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Management IRQ Select				Card Detect Enable	Ready Enable	Battery Warning Enable	Battery Dead Or Status Change Enable
RW:0000				RW:0	RW:0	RW:0	RW:0

Register Name: **Mapping Enable** *Register Per:* socket
Index: **06h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
I/O Map 1 Enable	I/O Map 0 Enable	MEMCS16 Full Decode	Memory Map 4 Enable	Memory Map 3 Enable	Memory Map 2 Enable	Memory Map 1 Enable	Memory Map 0 Enable
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

B.3 I/O Window Mapping Registers

Register Name: **I/O Window Control** *Register Per:* socket
Index: **07h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Timing Register Select 1	*Compatibility Bit*	Auto-Size I/O Window 1	I/O Window 1 Size	Timing Register Select 0	*Compatibility Bit*	Auto-Size I/O Window 0	I/O Window 0 Size
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Register Name: **System I/O Map 0–1 Start Address Low** *Register Per:* socket
Index: **08h, 0Ch** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 7:0							
RW:00000000							

Register Name: **System I/O Map 0–1 Start Address High** *Register Per:* socket
Index: **09h, 0Dh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 15:8							
RW:00000000							

Register Name: **System I/O Map 0–1 End Address Low** *Register Per:* socket
Index: **0Ah, 0Eh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 7:0							
RW:00000000							

Register Name: **System I/O Map 0–1 End Address High** *Register Per:* socket
Index: **0Bh, 0Fh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 15:8							
RW:00000000							

Register Name: **Card I/O Map 0–1 Offset Address Low** *Register Per:* socket
Index: **36h, 38h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 7:1							*0*[a]
RW:0000000							RW:0

[a] This bit must be programmed to '0'.

Register Name: **Card I/O Map 0–1 Offset Address High** *Register Per:* socket
Index: **37h, 39h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 15:8							
RW:00000000							

B.4 Memory Window Mapping Registers

Register Name: **System Memory Map 0–4 Start Address Low** *Register Per:* socket
Index: **10h, 18h, 20h, 28h, 30h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 19:12							
RW:00000000							

Register Name: **System Memory Map 0–4 Start Address High** *Register Per:* socket
Index: **11h, 19h, 21h, 29h, 31h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Window Data Size	*Compatibility Bit*	*Scratchpad Bits*		Start Address 23:20			
RW:0	RW:0	RW:00		RW:0000			

Register Name: **System Memory Map 0–4 End Address Low** *Register Per:* socket
Index: **12h, 1Ah, 22h, 2Ah, 32h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
End Address 19:12							
RW:00000000							

Register Name: **System Memory Map 0–4 End Address High** *Register Per:* socket
Index: **13h, 1Bh, 23h, 2Bh, 33h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Card Timer Select		*Scratchpad Bits*		End Address 23:20			
RW:00		RW:00		RW:0000			

Register Name: **Card Memory Map 0–4 Offset Address Low** *Register Per:* socket
Index: **14h, 1Ch, 24h, 2Ch, 34h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Offset Address 19:12							
RW:00000000							

Register Name: **Card Memory Map 0–4 Offset Address High** *Register Per:* socket
Index: **15h, 1Dh, 25h, 2Dh, 35h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write Protect	REG Setting	Offset Address 25:20					
RW:0	RW:0	RW:000000					

B.5 Extension Registers

Register Name: **Misc Control 1** *Register Per:* socket
Index: **16h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Inpack Enable	*Scratchpad Bits*		Speaker Enable	Pulse System IRQ	Pulse Management Interrupt	V_{CC} 3.3V	*Reserved*
RW:0	RW:00		RW:0	RW:0	RW:0	RW:0	R:X W:0

Register Name: **FIFO Control** *Register Per:* socket
Index: **17h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Empty Write FIFO	*Scratchpad Bits*[a]						
RW	RW:0000000						

[a] Because a write will fush the FIFO, these scratchpad bits should be used only when card activity is guaranteed not to occur.

Register Name: **Misc Control 2** *Register Per:* chip
Index: **1Eh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
IRQ15 Is RI Out	DMA System *(CL-PD6712/ CL-PD6722)*	Three-State Bit 7	Drive LED Enable	5V Core	Suspend	Low-Power Dynamic Mode	Bypass Frequency Synthesizer
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:1	RW:0

Register Name: **Chip Information** *Register Per:* chip
Index: **1Fh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Cirrus Logic Host-Adapter Identification		Dual/Single Socket*	CL-PD67XX Revision Level				*Reserved*
R:11		R:n[a]	R:nnnn[b]				R:n[c]

[a] The value for CL-PD6712 is '0', and the value for CL-PD6720 and CL-PD6722 is '1'.

[b] This read-only value depends on the revision level of the CL-PD67XX chip.

[c] The value for CL-PD6720 is '0', and the value for CL-PD6712 and CL-PD6722 is '1'.

Register Name: **ATA Control** *Register Per:* socket
Index: **26h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
A25/CSEL	A24/M/S*	A23/VU	A22	A21	*Scratchpad Bit*	Speaker Is LED Input	ATA Mode
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Register Name: **Extended Index** *Register Per:* socket
Index: **2Eh** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Extended Index							
RW:00000000							

Register Name: **Extended Data** *Register Per:* socket
Index: **2Fh** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Extended Data							

Register Name: **Data Mask 0** *Register Per:* socket
Index: **2Fh** *Extended Index:* **01h** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Mask Select 0							
RW:00000000							

Register Name: **Data Mask 1** *Register Per:* socket
Index: **2Fh** *Extended Index:* **02h** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Mask Select 1							
RW:00000000							

Register Name: **Extension Control 1** *Register Per:* socket
Index: **2Fh** *Extended Index:* **03h** *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMA Enable		Pull-up Control	*Reserved*		LED Activity Enable	Auto Power Clear Disable	V_{CC} Power Lock
RW:00		RW:0	RW:00		RW:0	RW:0	RW:0

Register Name: **Maximum DMA Acknowledge Delay** — *Register Per:* socket
Index: **2Fh** — *Extended Index:* **04h** — *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Maximum DMA Acknowledge Delay							
RW:00000000							

Register Name: **External Data** — *Register Per:* socket
Index: **2Fh** — *Extended Index:* **0Ah** — *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
External Data 7	External Data 6	External Data 5	External Data 4	External Data 3	External Data 2	External Data 1	External Data 0
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Register Name: **External Data** — *Register Per:* socket
Index: **6Fh** — *Extended Index:* **0Ah** — *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
External Data 7	External Data 6	External Data 5	External Data 4	External Data 3 or B_VS2 Input	External Data 2 or B_VS1 Input	External Data 1 or A_VS2 Input	External Data 0 or A_VS1 Input
RW:0	RW:0	RW:0	RW:0	R:0	R:0	R:0	R:0

Register Name: **Extension Control 2** — *Register Per:* socket
Index: **2Fh and 6Fh** — *Extended Index:* **0Bh** — *Register Compatibility Type:* ext.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Active-high GPSTB	GPSTB on IOW*	GPSTB on IOR*	Totem-pole GPSTB	*Reserved*	
RW:00		RW:0	RW:0	RW:0	RW:0	RW:00	

B.6 Timing Registers

Register Name: **Setup Timing 0–1**							*Register Per:* socket
Index: **3Ah, 3Dh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Setup Prescalar Select		Setup Multiplier Value					
RW:00		RW:000001					

Register Name: **Command Timing 0–1**							*Register Per:* socket
Index: **3Bh, 3Eh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Command Prescalar Select		Command Multiplier Value					
RW:00		RW:000110/001111[a]					

[a] Timing set 0 (index 3Bh) resets to 06h for socket timing equal to standard AT-bus-based cycle times. Timing set 1 (3Eh) resets to 0Fh for socket timings equal to standard AT-bus timing using one additional wait state.

Register Name: **Recovery Timing 0–1**							*Register Per:* socket
Index: **3Ch, 3Fh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Recovery Prescalar Select		Recovery Multiplier Value					
RW:00		RW:000011					

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