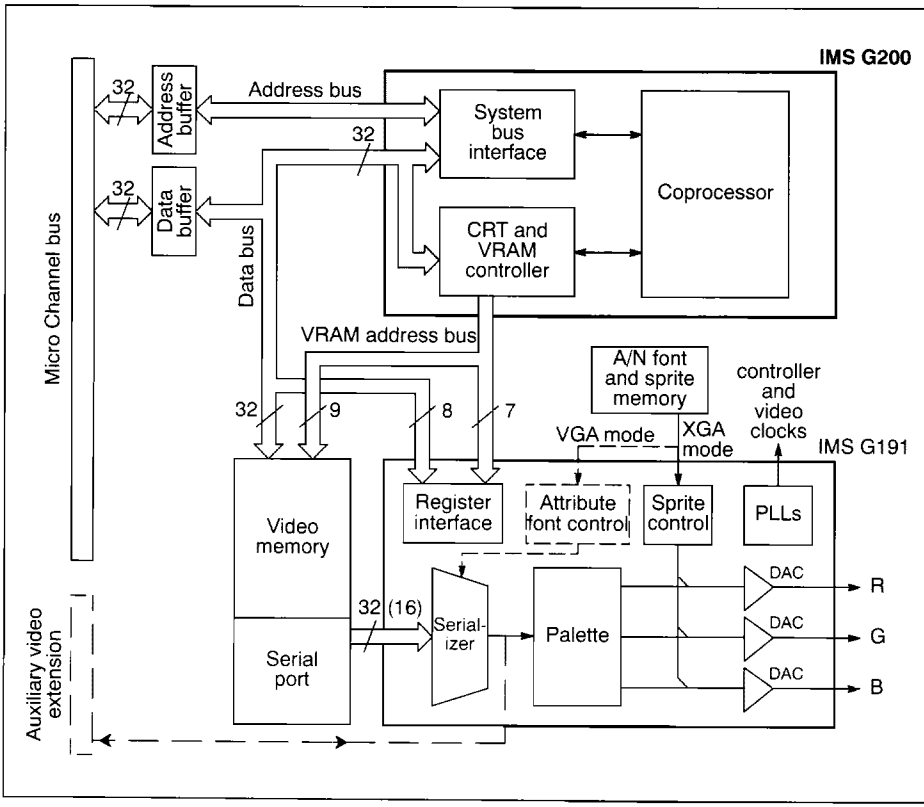
XGA DISPLAY CONTROLLER



FEATURES

VGA and XGA standard registers
Programmable CRT controller supports many display modes including:
- 1280×1024 with 256 colors (interlaced),
- 800×600 with 65,536 colors (non-interlaced)
- 1024×768 with 256 colors (non-interlaced),

132 column text mode supports 1056×480 resolution
16 bit true color support (5 Red, 6 Green, 5 Blue)
Video RAM interface for high performance
Supports and interfaces to Micro Channel bus
Bus mastership on the Micro Channel bus

IMS G200 coprocessor supports:
- 1, 2, 4, 8 and 16 bit Pixel and bit block transfers
- Line drawing
- Area filling
- Logical and arithmetic pixel mixing
- Pixel map masking
- Scissoring
- X, Y axis addressing

TABLE OF CONTENTS

21.1 Detailed IMS G200 block diagram

The IMS G200 display controller chip comprises the system bus interface, drawing coprocessor, and the memory and display controller components of an XGA subsystem based on the G201/G191 chipset.

Figure 21.1 shows the main functional units of the IMS G200 with all pin connections. The following sections of this document include pin details and give a full description of each of the functional units which make up the IMS G200.

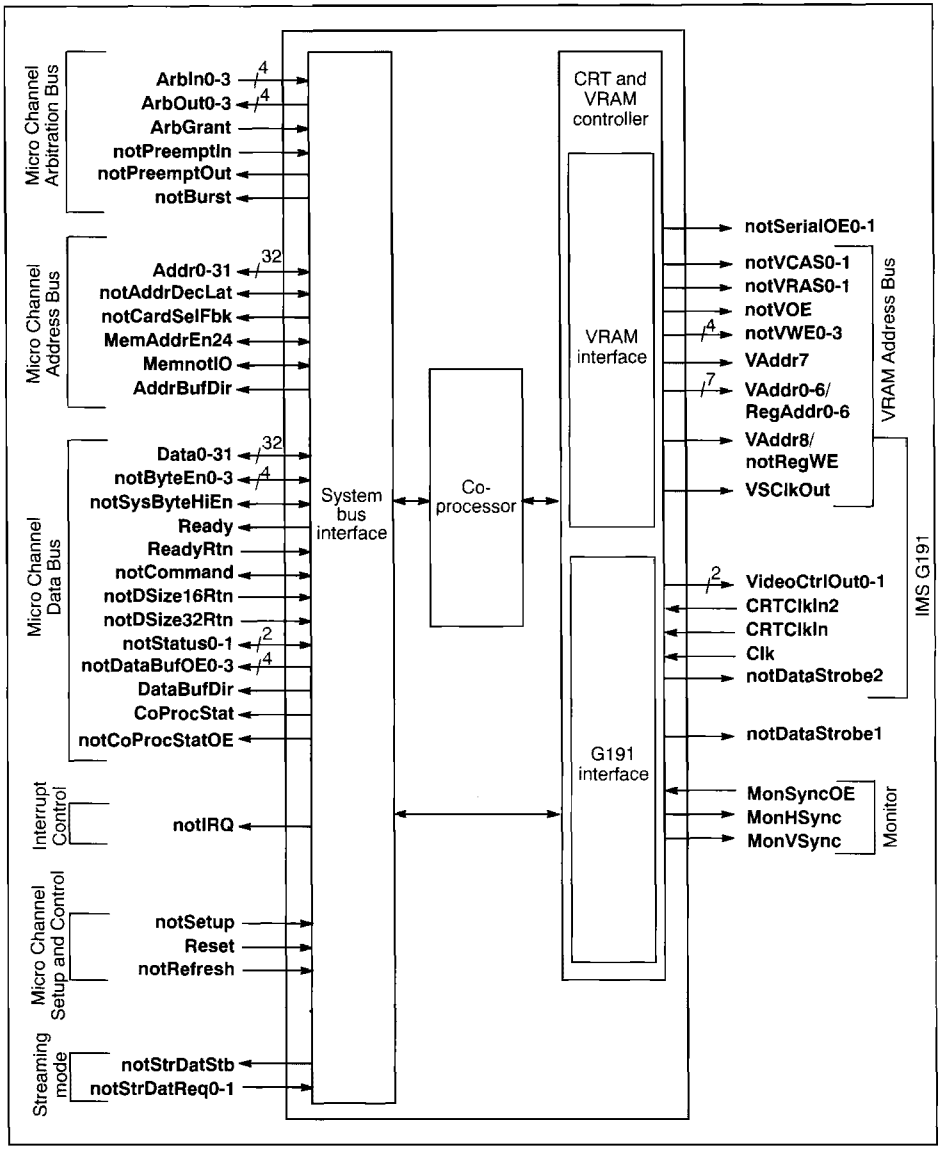


Figure 21.1 IMS G200 block diagram

21.2 Pin function reference guide

Signal names are prefixed by **not** if they are active low, otherwise they are active high. For a full description of the functions of the Micro Channel pins refer to the *IBM PS/2 hardware technical reference manual*.

21.2.1 Micro Channel bus interface

Address bus

Pin name	I/O	Signal description
Addr0-31	I/O	Address bus to communicate with the Micro Channel address bus. **Addr0** is the least significant bit (LSB) and **Addr31** is the most significant bit (MSB). These lines must be buffered externally to meet minimum drive requirements of the Micro Channel.
MemAddrEn24	I/O	Memory address enable 24 bits. This line indicates when an extended address is used on the bus. When **MemAddrEn24** is active this indicates that an unextended 24 bit address for less than or equal to 16 Mbytes is being presented.
notCardSelFbk	O	Card selected feedback. When the controlling master (e.g. i386 processor) addresses the G200, the G200 drives **notCardSelFbk** active to indicate its presence at the address specified.
notAddrDecLat	I/O	Address decode latch.
MemnotIO	I/O	Pin to distinguish between a memory cycle and an input/output (I/O) cycle. When **MemnotIO** is high a memory cycle is in progress, when low an I/O is in progress.
AddrBufDir	O	This signal controls the direction of an external 3 state bidirectional buffer isolating the IMS G200 from the Micro Channel address bus. A high signifies the Micro Channel bus is driving the IMS G200 pins (G200 is the slave), a low signifies that the IMS G200 is driving the Micro Channel bus (G200 is the master).

Arbitration bus

Pin name	I/O	Signal description
ArbOut0-3	O	These outputs drive the Micro Channel arbitration bus priority levels. These signals must be buffered by an open collector device to meet Micro Channel requirements.
ArbIn0-3	I	These inputs are the Arbitration bits from the Micro Channel bus to enable the IMS G200 to control the bus in bus master mode.
ArbGrant	I	Arbitration grant signal.
notPreemptOut	O	This is the output portion of the Micro Channel **–PREEMPT** signal. This signal must be buffered by an open collector or three-state device to comply with Micro Channel convention.
notPreemptIn	I	**notPreemptIn** is logically tied directly to the Micro Channel **–PREEMPT** signal. This signal in conjunction with **notPreemptOut** mimics the open collector driver specified for **–PREEMPT** in the Micro Channel definition. It is used when the IMS G200 is operating in bus master mode.
notBurst	O	This signal indicates to the central arbitration control point the extended use of the channel for transferring a block of data. This type of data transfer is called a burst cycle.

Data bus

Pin name	I/O	Signal description
Data0-31	I/O	Data bits 0 to 31. **Data0** is the LSB and **Data31** is the MSB. The data pins are shared by the VRAM random data port and the Micro Channel data bus. They may connect directly to the VRAM but must be isolated from the Micro Channel by suitable bidirectional three-state drivers.
Data8-11		**Data8-11** are also used to carry an address for external registers.
Data8-20		**Data8-20** are also used to carry an address for external memory (typically EPROM).
Data27		**Data27** (with **notDataStrobe1**) is also a strobe qualifier for chip configuration data.
Data28		**Data28** is also a strobe qualifier for writes to external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory write.
Data29		**Data29** is also a strobe qualifier for reads from external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory read.
Data30		**Data30** is also a strobe qualifier for external register writes. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register write.
Data31		**Data31** is also a strobe qualifier for external register reads. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register read.
DataBufDir	O	This signal controls the direction of an external bidirectional three state transceiver isolating the Micro Channel data bus from the shared VRAM data bus. A low indicates drive towards the Micro Channel data bus. A high indicates drive towards the IMS G200 and VRAM.
notDataBufOE0-3	O	A low on this signal puts the external Micro Channel data bus isolation buffer in the active state; a high puts it in high impedance state. Bit 0 controls data bus bits 0:7, bit 1 controls data bus bits 8:15, bit 2 controls data bus bits 16:23, and bit 3 controls data bus bits 24:31.
notCommand	I/O	This signal is used to define when data is valid on the data bus.
Ready	O	This normally active signal is pulled inactive (not ready) by the IMS G200 to allow additional time to complete a Micro Channel operation.
ReadyRtn	I	A positive AND of all the Micro Channel CD CHRDY (Ready) signals.
CoProcStat	O	The **CoProcStat** pin is an external output of bit 7 (BSY) of the Auxiliary Coprocessor Control Register (offset 11 in coprocessor address space). This provides an additional method of reading the coprocessor busy status without halting its operation (as would happen if the status was read via the coprocessor data bus). **CoProcStat** should be connected through a tri-state buffer to **Data15 (or Data7** on an 8-bit bus).
notCoProcStatOE	O	This pin provides the enable input for the tri-state buffer that connects the **CoProcStat** pin to bit 15 of the host data bus (host side of the data buffer's transceivers).

Pin name	I/O	Signal description
notStatus0-1	I/O	Status bits 0 and 1. These lines indicate the start of a cycle and also define the type of cycle. Used in conjunction with the **MemnotIO** pin memory read/write operations are distinguished from I/O read/write operations as defined below:
notDSize16Rtn	I	Data size 16 bits return. This signal is provided to allow the controlling master to monitor the data size information.
notDSize32Rtn	I	Data size 32 bits return. This signal is provided to allow the controlling master to monitor the data size information.
notSysByteHiEn	I/O	System byte high enable. This line indicates and enables transfer of data on the high byte of the data bus (**Data8-15**) and is used with **Addr0** to distinguish between high byte transfers (**Data8-15**) and low byte transfers (**Data0-7**).
notByteEn0-3	I/O	Byte enables (used in conjunction with 32-bit bus cycles).

MemnotIO	notStatus0	notStatus1	Function
0	0	1	I/O write
0	1	0	I/O read
1	0	1	memory write
1	1	0	memory read

Interrupt control

Pin name	I/O	Signal description
notIRQ	O	Interrupt request

Setup and control

Pin name	I/O	Signal description
notRefresh	I	This signal is used to indicate a memory refresh operation is in progress.
notSetup	I	Micro Channel bus setup
Reset	I	Bus reset
Clk	I	Clock

Streaming mode

Pin name	I/O	Signal description
notStrDatStb	O	Connects to the Micro Channel –SD STB signal. **notStrDatStb** is driven by the IMS G200 (acting as the bus master) and serves as a clock, delimiting words in a streaming data transfer.
notStrDatReq0-1	I	Connects to the Micro Channel –SDR(0,1) signals. –SDR(0,1) are driven by the bus slave, following the activation of the Address Data Latch signal, to indicate that it supports streaming data.

21.2.2 VRAM interface

Pin name	I/O	Signal description
VAddr0-8	O	These pins have different functions depending on the operation. **VAddr0-8** carry the row and column addresses to the VRAM's to be strobed by the appropriate **RAS** or **CAS** signal. **VAddr0-6** lines are also used to send the address of the IMS G191 parameter registers to the IMS G191. **VAddr8** is also used as a **notRegWE** pin to indicate to the IMS G191 whether the IMS G191 addressed register is being written to or read from. A high on this signal indicates a read from the register, a low indicates a write to the register.
VAddr0-6		
VAddr8 / notRegWE		
notSerialOE0-1	O	Serial output enable strobes for multiplexing data from any one of four VRAM serial ports.
notVCAS0-1	O	VRAM column address strobes.
notVRAS0-1	O	VRAM row address strobes.
notVWE0-3	O	Write Enable control for VRAM data. A low indicates a write operation. Bit 0 controls **Data 0-7** Bit 1 controls **Data 8-15** Bit 2 controls **Data 16-23** Bit 3 controls **Data 24-31**
notVOE	O	This signal connects to the **TRANSFER/OUTPUT ENABLE** of the VRAM. It enables the VRAM outputs at the appropriate times as well as defining serializer load cycles to the VRAM.
VSClkOut	O	This signal causes shift cycles on the VRAM serial ports. The IMS G200 controls the shift timing based on bits per pixel and prescaling of the master clock source from the IMS G191.

21.2.3 IMS G191 interface

Pin name	I/O	Signal description
VideoCtrlOut0-1	O	These pins represent the horizontal scan line state. Table 21.8 (page 429) shows the decoding of the bits.
notDataStrobe2	O	This signal is used to strobe data from the IMS G200 to the IMS G191. It is used to communicate register contents programmed by the host processor and decoded in the IMS G200. A low sent on this pin to the IMS G191 indicates that the IMS G191 should perform the action defined by the **VAddr0-6** and **notRegWE** pins.
CRTClkIn **CRTClkIn2**	I I	CRTC clocks. These clocks are sourced by the IMS G191 and are used by the IMS G200 to generate all video related timings.
MonHSync	O	This is the monitor horizontal sync pulse. It can be programmed to pulse either positive or negative. It enters the high impedance state when **MonSyncOE** is high.
MonVSync	O	This is the monitor vertical sync pulse. It can be programmed to pulse either positive or negative. It enters the high impedance state when **MonSyncOE** is high.
MonSyncOE	I	A low on this input will cause the **MonHSync** and **MonVSync** to three-state their outputs.

21.2.4 Supplies

Pin name	I/O	Signal description
VDD		VDD
GND		GND

21.2.5 Miscellaneous

Pin name	I/O	Signal description
notDataStrobe1	O	This signal strobes low to cause reads and writes to/from the external memory (typically PROM) and external registers.
HoldToGND		Must be connected to **GND**
HoldToVDD		Must be connected to **VDD**
N/C		No Connect (this refers to unused pins). Do not wire this pin.

21.3 Coprocessor

The coprocessor provides hardware drawing assist functions. These functions can be performed on graphics data in both video memory and system memory.

The coprocessor updates memory independent of the system microprocessor. A virtual memory feature allows the coprocessor to perform linear to physical address conversion in a manner consistent with the paging operation in the 80X86 processor family. The instructions are written to a set of memory-mapped registers (see Section 21.7.1); the coprocessor then executes the drawing function.

The coprocessor functions are summarized below:

- Pixel Block Transfer (PxBlt) - This function provides a four term block transfer capability of an entire bit map, or part of a bit map, from one location to another. This transfer can be: within video memory, within system memory, or between system and video memory.
- Line draw - This function draws lines, with a programmable style, into a bit map in video memory or system memory.
- Area fill - This function fills an outlined area with a programmable pattern. It can be performed on an area outline in video or system memory.
- Logical and arithmetic pixel mixes - These functions provide logical and arithmetic operators that can be used against data in video or system memory.
- Scissoring - This function provides a rectangular mask function, which can be used instead of the mask map.
- Map masking - This function provides control over updates to each pixel for all drawing functions.
- X, Y addressing - This function allows a pixel to be specified by its X and Y coordinates within a pixel map, instead of its linear address in memory.
- Virtual addressing - When enabled, this function causes the coprocessor function to utilize a page table of a form identical to the 80X86 processor family page table. A translation look aside buffer is kept on chip to speed conversion of addresses.

21.3.1 Pixels, pixel maps and X, Y addressing

The drawing coprocessor works on pixels within pixel maps. A pixel map is an area of memory at a given address (the base address) with a defined width, height and pixel format. Pixels can have 1, 2, 4, 8 or 16 bits. The pixels can be ordered within bytes in one of two ways: left to right or vice versa. The XGA allows pixel maps of any arbitrary size up to 4096×4096 pixels.

The coprocessor is programmed using X, Y coordinates that are automatically converted into linear memory addresses (using the defined width and pixel size) before accessing the physical memory (see Figure 21.2).

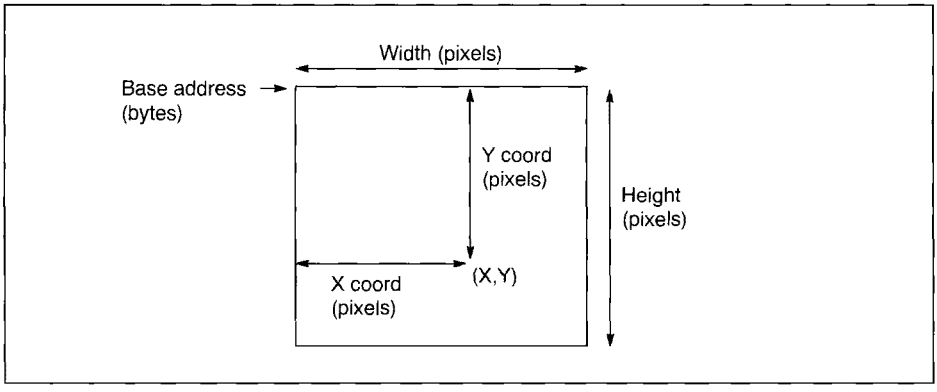


Figure 21.2 Pixels are addressed using X,Y coordinates within pixel maps

The programmer can define up to four pixel maps at one time. Three maps (A, B and C) are general purpose; the other is always used as the mask map. When starting a drawing operation, the programmer tells the coprocessor which maps are to be used as the source, the pattern, and the destination. In this way, map A, for example, could be the display pixel map. It could then be used as source, destination, or both, without having to move the pixel map parameters from one set of registers to another.

21.3.2 Pixel maps in system memory

A certain amount of space is available in the non-displayed (off-screen) areas of video memory. This is often used for storing fonts and off-screen pixel maps. GUIs, however, make extensive use of off-screen pixel maps (for example, for pull-down menus), and may be called upon to use fonts that are too large to fit in off-screen video memory. When the off-screen video memory is full, the GUI device driver can use normal system memory. With previous adapters, this generally meant processing the pixels using the system processor which is slow compared to special drawing hardware, especially if the operation is not a simple copy. It also ties up the processor and prevents it from preparing for the next drawing operation.

The XGA uses bus-mastership on the Micro Channel to overcome these problems. The drawing coprocessor's power can be used on pixel data anywhere in system or video memory.

To support paged memory environments, where the paging unit in the 80386 or 80486 is turned on, the XGA includes its own paging unit, using page tables of the same form. The XGA can operate using the main page tables used by the operating environment (with its cooperation), or on tables built by device drivers or applications themselves.

21.3.3 Pixel block transfer (PxBlt)

The PxBlt function works with four operands: the source, pattern, destination and mask. The source may come from a pixel map to copy data, or from color registers to set the destination to a particular color. The pattern may come from a pixel map, indirectly from the source, or it may be disabled.

For each pixel, the source and destination are combined using a Mix function selected by the 1-bit-per-pixel pattern. A 0 in the pattern selects the background mix, and a 1 selects the foreground mix. A full set of logical mixes is provided, supporting all the OS/2 and Windows Raster Operations (ROPs), with a selection of arithmetic mixes. Fast text drawing is crucial to windowing environments and other interactive applications. The pattern can select between foreground and background colors, allowing a 1-bit-per-pixel text font in the pattern map to be rapidly expanded to colored characters in the destination.

The pattern and the source have another common feature. The X, Y addresses for these maps automatically wrap when they reach either side or top and bottom. This allows a small pattern to be "tiled" over a large area in the destination using a single operation (see Figure 21.3).

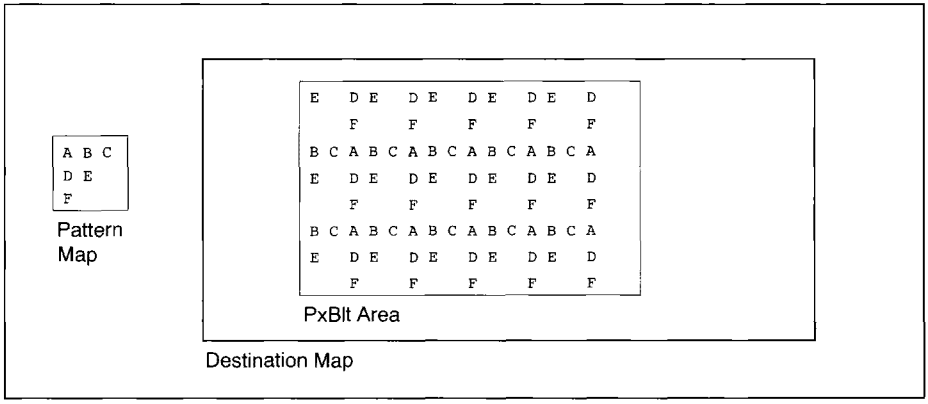


Figure 21.3 Patterns are automatically tiled

21.3.4 Lines

The coprocessor draws lines using the Bresenham line-drawing algorithm. All pixels of a line can be drawn, or the first or last pixel can be suppressed to draw poly lines correctly.

As with PxBlt, the pattern and source X, Y coordinates wrap at the edge of the maps. Line drawing, however, is different. While the X, Y coordinates of the destination move along the required path, the coordinates in the source and pattern move horizontally - left to right only. A simple 1-pixel-high pattern is drawn along the line, as shown in Figure 21.4.

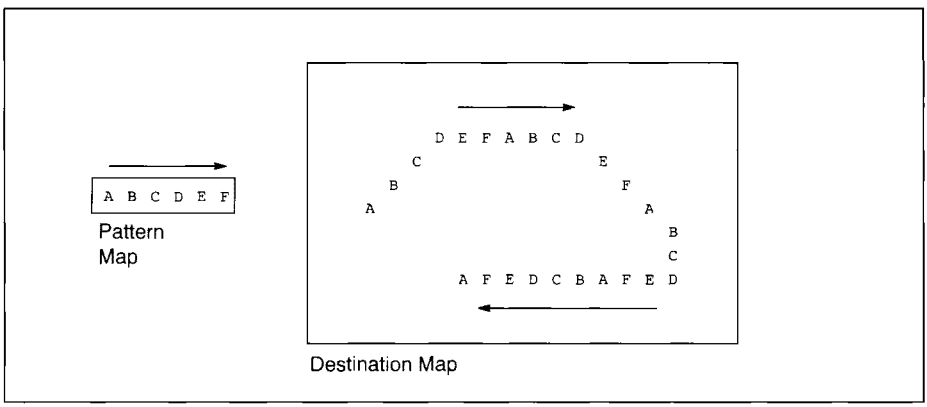


Figure 21.4 Line patterns are also pixel maps

Short lines can be drawn with simpler commands using 'short stroke vectors', line segments up to 16 pixels long, and in one of eight directions (the X axis, the Y axis and the 45° lines in between).

21.3.5 Area fill

The coprocessor allows arbitrary areas to be filled rapidly. The area is defined by an outline drawn in a 1-bit-per-pixel map. The outline is drawn using special versions of the line drawing functions (including short strokes).

When the outline is complete, a special PxBlt fills the inside of the defined figure. A parity fill algorithm is used, where a rectangle is scanned from left to right, starting from outside the figure, and alternately moving in and out of the figure as each successive boundary is crossed. The area can also be filled with a pattern if required.

21.3.6 Scissoring and map masking

The coprocessor can, under programmer control, automatically 'scissor' (that is, not draw) pixels that an operation attempts to draw outside a specified area. That area can be a simple rectangle, or a more complex shape defined in a pixel map (the mask map), with a pattern of 1's and 0's (1 allows the corresponding pixel in the destination to be changed; a 0 protects that pixel). This function can be used, for example, when drawing into a background window that is partially obscured by other windows.

21.3.7 State save and restore

In a multi-tasking environment, the system processor must change tasks from time to time. When changing tasks, the state of the current task must be saved so that it can be restored and continued at a later time. The state of the coprocessor can be rapidly saved and restored, making multi-tasking operation possible.

The coprocessor's operation can be suspended at any time and later resumed. Once suspended, the entire state of the coprocessor, including internal registers not visible in the address space, can be saved to memory by reading repeatedly from two 32 bit I/O ports. The 80X86 string input (INS) instruction can be used for this. The state is restored by writing the previously saved state data back into the same ports (using the OUTS instruction). Once resumed, the operation will continue from exactly the point at which it was suspended.

21.4 System bus interface

This portion of the IMS G200 display controller provides control of the interface between the video subsystem and the system microprocessor. It decodes the addresses for VGA and XGA I/O registers and the memory addresses for the coprocessor memory-mapped registers and video memory. It also provides controls that allow access to: registers in the IMS G191 serializer palette DAC, data in the sprite memory, ROM, and external registers.

It also provides the bus-master function and determines whether the system data bus is 16 or 32 bits wide.

The system bus interface is designed to interface to the Micro Channel. It provides buffer controls so that high current drivers can be supplied in external packages. In some instances where open collector outputs are required, the IMS G200 display controller provides separate inputs and outputs that connect to the driver input and output. The arbitration (ARB) signals on the Micro Channel are examples.

21.5 CRT and VRAM controller

The memory controller controls accessing of the VRAM. It supports memory either 16 or 32 bits wide. The minimum implementation is 512 Kbytes.

The CRT controller (CRTC) generates all the timing signals required to drive the serializer and the display. It consists of two counters, one for horizontal parameters, and one for vertical parameters, and a series of registers. The counters run continuously, and when the count value reaches that specified in one of the associated registers, the event controlled by that register occurs.

21.5.1 Extended mode CRT controller register interpretations

A pictorial representation of the function of each of the CRT controller registers is shown in Figure 21.5.

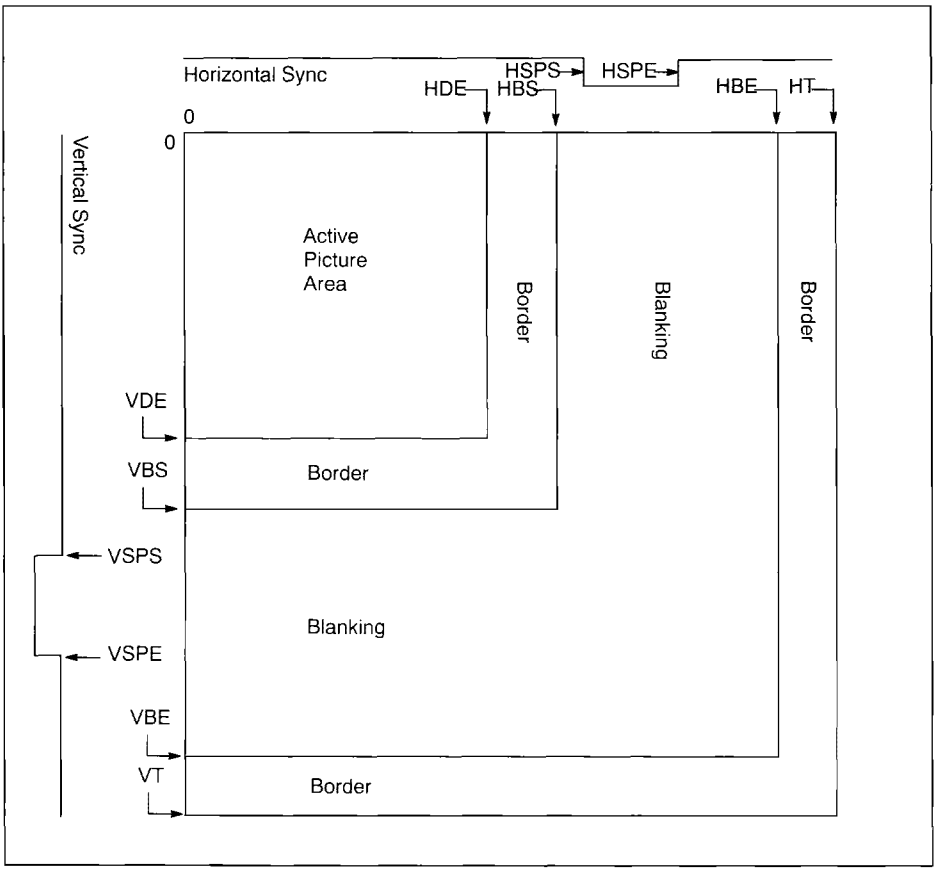


Figure 21.5 CRT controller register definitions

Horizontal scan registers		Vertical scan registers	
HT	Horizontal total register	**VT**	Vertical total register
HDE	Horizontal display end register	**VDE**	Vertical display end register
HBS	Horizontal blanking start register	**VBS**	Vertical blanking start register
HBE	Horizontal blanking end register	**VBE**	Vertical blanking end register
HSPS	Horizontal sync pulse start register	**VSPS**	Vertical sync pulse start register
HSPE	Horizontal sync pulse end register	**VSPE**	Vertical sync pulse end register

Table 21.1 Registers which control a horizontal and a vertical scan of the display

The XGA can be programmed to inform the host processor of the start and the end of the Active Picture Area using a system interrupt. An enable and a status bit exist for each interrupt.

21.6 XGA I/O-mapped and memory-mapped registers

XGA is controlled using a combination of I/O-mapped and memory-mapped registers. I/O-mapped registers are those that appear in the I/O address space of an 80X86 processor, and are accessed using IN, OUT, or other I/O instructions. Memory-mapped registers appear in the memory address space of an 80X86 processor, and are accessed using standard memory operations with all the available combinations of registers and addressing modes. In addition, many I/O-mapped registers are indexed (that is, the register is selected using an index in one I/O port, and the data for all indexed registers is written through a second I/O port). This technique, used also by the VGA, reduces the I/O address space required.

Memory-mapped registers are generally used to control the drawing coprocessor, where frequent access requires good performance. I/O-mapped registers (indexed and direct) are used for the remainder (mainly setup registers, where performance is less important). Table 21.2 shows the XGA direct access I/O registers.

Multiple XGA adapters (multiple instances) can be used in a system. Each instance has an instance number and has its registers mapped at different addresses. The memory-mapped registers are located at some point within the address range C0000 and DFFFF. The precise location is set by a system dependent configuration process, such as the PS/2 Micro Channel auto-configuration. Figures 21.6 and 21.7 illustrate how the I/O and memory-mapped registers are located. When multiple XGA subsystems are installed in a system, the memory-mapped registers for all instances can be mapped within the same 8 Kbyte block of address space. The allocation of addresses is the responsibility of the system configuration process, which ensures that there is no conflict between installed adapters (XGA or others).

Base address of the sixteen I/O registers of an XGA is 21x0, where x is the instance number. Figure 21.6 shows instance 6.

Base address of the memory-mapped registers of an XGA is (ROM Base address) + 7K + (128×instance number). Figure 21.7 shows instance 6.

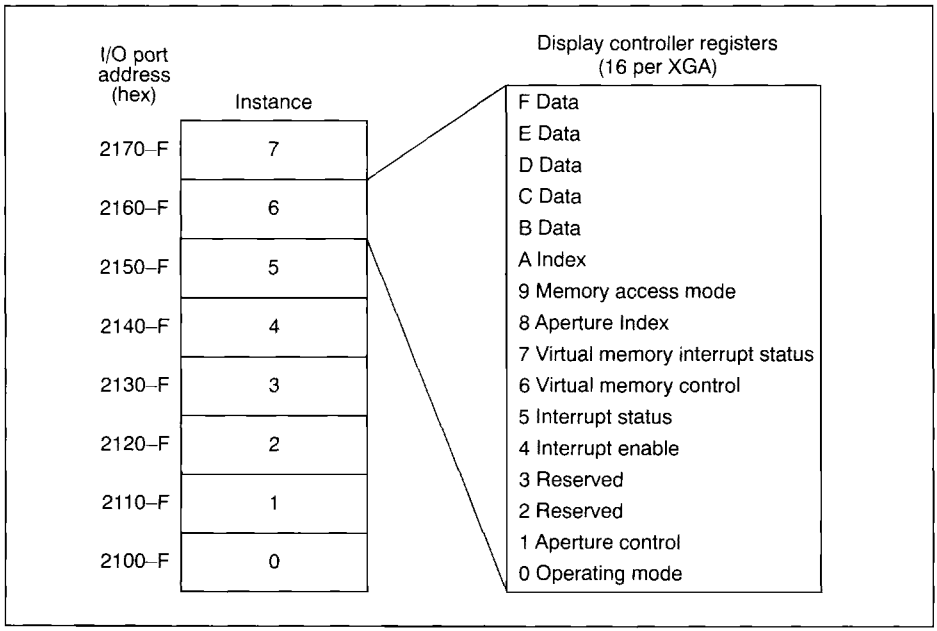


Figure 21.6 I/O port addressing of XGA registers

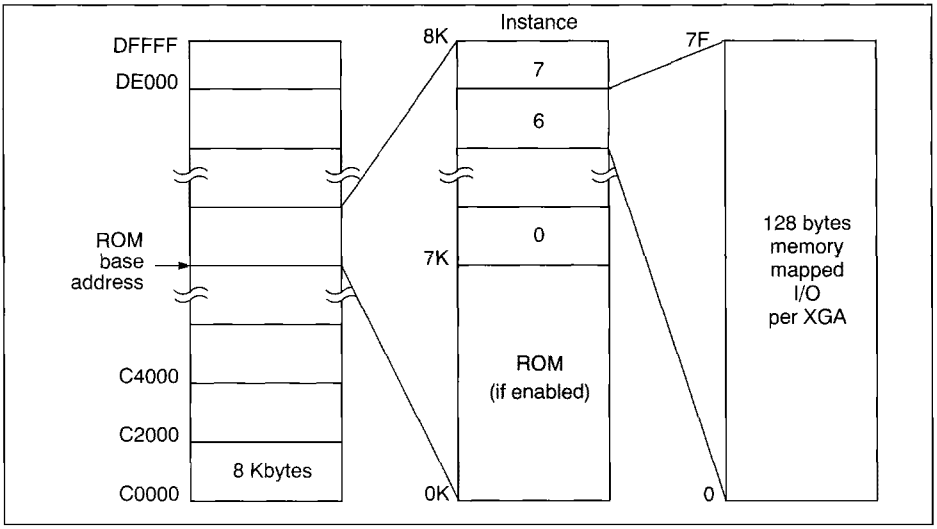


Figure 21.7 Memory mapped addressing of XGA registers

I/O port address	Register	Read/ Write	Description
21x0	Operating mode	R/W	Defines display mode (VGA, 132 or XGA)
21x1	Aperture control	R/W	Controls a 64K aperture through which the XGA memory can be accessed in the system address space. This window gives real mode applications and operating systems a means of accessing the XGA video memory.
21x2			Reserved
21x3			Reserved
21x4	Interrupt enable	R/W	Contains bits to enable/disable the interrupt conditions that can be generated by the subsystem.
21x5	Interrupt status	R/W	Indicates the interrupt status bits that can be generated by the subsystem and used to reset the corresponding interrupts.
21x6	Virtual memory control	R/W	This register is directly mapped to the I/O address space.
21x7	Virtual memory interrupt status	R/W	This register is directly mapped to the I/O address space.
21x8	Aperture index	R/W	Used to provide address bits to the video memory when the aperture in system address space being used is smaller than the amount of video memory installed.
21x9	Memory access mode	R/W	Controls pixel ordering when the video memory is being accessed by the system (not the coprocessor). Intel or Motorola order can be selected. This register also controls the number of bits per pixel.

I/O port address	Register	Read/ Write	Description
21xA	Index	R/W	Selects which indexed Extended Graphics Mode register is accessed when any address (base+B) to (base+F) is read or written.
21xB 21xC 21xD 21xE 21xF	Data	R/W	These registers are used when reading and writing to the register indexed by the Index register (21xA). The read/ write operation can be of byte, word, or double-word size using these data registers.

Table 21.2 XGA direct access I/O registers

Traditionally, display adapters such as the VGA and the 8514/A have been controlled through registers mapped into the 80X86 I/O address space. Memory-mapped registers have been introduced in the XGA for controlling the drawing coprocessor, where accesses are frequent and good performance is essential.

The I/O address space in the 80X86 is limited to 64 Kbytes, so individual adapters can only use a restricted number of addresses (to avoid possible conflicts between adapters). When the adapter contains many registers (typical of a display controller), indexed register addressing schemes are often used, as noted above. Memory address space is much larger (1 Mbyte minimum in real mode), so adapters with memory-mapped registers can avoid using indexing, thus allowing direct access to all registers, and reducing code space and execution time.

When the 80386 is running in Protected mode, the processor normally checks I/O accesses by applications to ensure they are allowed. It reads the I/O Permission Bitmap, a process that adds twenty cycles to each individual I/O access. Memory-mapped registers avoid this overhead, reducing to one-tenth the time taken to start many graphics operations.

Another advantage relates to multiple display adapters. Each instance of the XGA has a different set of register addresses, as shown earlier. Software must be able to run with any possible set. The 80X86 allows base-plus-offset addressing for memory accesses, using a segment register and an immediate or register-based offset. The software would typically set the segment register to point to the first address of the memory-mapped registers, and then have immediate pointers to specific registers. I/O addresses, on the other hand, are always contained in the DX register of an 80X86 processor; no form of base-plus-offset addressing is possible. For I/O-mapped registers, DX must be calculated correctly before each access, taking time and code space.

21.7 IMS G200 register reference guide

The following section lists all the IMS G200 registers with a brief description of the function of each register. The complete register bit format is not included in this datasheet, this is defined in the *XGA Software Programmer's Guide*, document number 72 OEK 258 01. All addresses and indexes are in hexadecimal. Unspecified registers, or registers marked as 'RESERVED', are reserved and must not be written to or read from.

21.7.1 IMS G200 memory mapped registers

The IMS G200 coprocessor is controlled using a bank of 128 memory mapped registers. Table 21.3 shows the register memory map for the IMS G200 coprocessor in Intel register format. The register descriptions are given in Table 21.4.

Byte 3	Byte 2	Byte 1	Byte 0	
Page Directory Base Address				0
Current Virtual Address				4
RESERVED		Auxiliary Coprocessor Control	RESERVED	8
RESERVED		State B len	State A len	C
RESERVED	Pixel Map Index	Coprocessor Control	RESERVED	10
Pixel Map n Base Pointer				14
Pixel Map n Height		Pixel Map n Width		18
RESERVED			Pixel Map n Format	1C
RESERVED		Bresenham Error Term		20
RESERVED		Bresenham K1		24
RESERVED		Bresenham K2		28
Direction Steps				2C
RESERVED				30
RESERVED				34
RESERVED				38
RESERVED				3C
RESERVED				40
RESERVED				44
RESERVED	Dest Color Comp. Cond.	Bgd Mix	Fgd Mix	48
Destination Color Compare Value				4C
Pixel Bit Mask				50
Carry Chain Mask				54
Foreground Color Register				58
Background Color Register				5C
Operation Dimension 2		Operation Dimension 1		60
RESERVED				64
RESERVED				68
Mask Map Origin Y Offset		Mask Map Origin X Offset		6C
Source Map Y Adr		Source Map X Adr		70
Pattern Map Y Adr		Pattern Map X Adr		74
Dest. Map Y Adr		Dest. Map X Adr		78
Pixel Operation				7C

Table 21.3 IMS G200 coprocessor register memory map

Off-set	Register	Read/ Write	Description
0	Page Directory Base Address	Write	Contains a 20 bit pointer to the page in physical memory containing the current Page Directory for the current task.
4	Current Virtual Address	Read	Contains the faulting page address in the event of a 'Not Present' or 'Protection Interrupt' being flagged.
9	Auxiliary Coprocessor Control	Read	Contains a duplicate status bit to the Coprocessor Busy bit (BSy, bit 7) of the Coprocessor Control register. The state of this bit is provided on the **CoProcStat** pin, enabling the busy status to be read without halting the coprocessor.
C D	State A len State B len	Read	These registers return the length, in double words, of the two parts, A and B of the coprocessor state for save and restore.
11	Coprocessor Control	R/W	Indicates if the coprocessor is currently executing an operation. In addition, the current coprocessor operation can be terminated or suspended by writing to this register.
12	Pixel Map Index	Write	Selects which of the pixel maps (A, B, C or mask) the four pixel map description registers apply.
14	Pixel Map n Base Pointer	Write	Specifies the byte address in memory of the start of a pixel map. If virtual address mode is enabled this address is a virtual address, otherwise it is a physical address.
18	Pixel Map n Width	Write	Specifies the width in pixels of a pixel map.
1A	Pixel Map n Height	Write	Specifies the height in pixels of a pixel map.
1C	Pixel Map n Format	Write	Specifies the format of a pixel map (Intel or Motorola) and the size of a pixel map in bits/pixel.
20	Bresenham Error Term	R/W	Specifies the Bresenham Error Term (E) for the draw line function.
24	Bresenham K1	Write	Specifies the Bresenham Constant (K1) for the draw line function.
28	Bresenham K2	Write	Specifies the Bresenham Constant (K2) for the draw line function.
2C	Direction Steps	Write	Used to specify up to 4 draw and step codes to the coprocessor and to initiate a draw and step operation.
48	Fgd Mix	Write	Holds the foreground mix value that specifies a logic or arithmetic function to be performed between the Destination and Function 1 second operand pixels during an operation where the Pattern pixel value is 1.
49	Bgd Mix	Write	Holds the background mix value that specifies a logic or arithmetic function to be performed between the Destination and Function 0 second operand pixels during an operation where the Pattern pixel value is 0.
4A	Dest Color Comp. Cond.	Write	Specifies the destination color compare condition under which destination update is inhibited.
4C	Destination Color Compare Value	Write	Contains the comparison value with which the destination pixels are compared when color compare is enabled.
50	Pixel Bit Mask	Write	Specifies which bits within each pixel are to be updated by the coprocessor.

Off-set	Register	Read/ Write	Description
54	Carry Chain Mask	Write	Contains a mask up to 31 bits wide. The mask is used to specify how the carry chain of the ALU is propagated when performing arithmetic update mixes and color compare operations.
58	Foreground Color Register	Write	Holds the foreground color to be used during coprocessor operations. The foreground color can be specified as the Foreground Source by setting up the appropriate field in the Pixel Operation Register.
5C	Background Color Register	Write	Holds the background color to be used during coprocessor operations. The background color can be specified as the Background Source by setting up the appropriate field in the Pixel Operation Register.
60	Operation Dimension 1	Write	Specifies the width of the rectangle to be drawn by the PxBlt function, or the length of the line in a line draw operation.
62	Operation Dimension 2	Write	Specifies the height of the rectangle to be drawn by the PxBlt function.
6C 6C	Mask Map Origin X Offset Mask Map Origin Y Offset	Write	These registers specify the X and Y offset of the Mask Map origin relative to the origin of the Destination Map.
70 72	Source Map X Adr Source Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Source pixel.
74 76	Pattern Map X Adr Pattern Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Pattern pixel.
78 7A	Dest. Map X Adr Dest. Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Destination pixel.
7C	Pixel Operation	Write	It is used to define the flow of data during an operation, specifies the address update function that is to be performed, and initiates PxBlt and Line Draw operations.

Table 21.4 IMS G200 coprocessor memory mapped register descriptions

21.7.2 IMS G200 XGA indexed access I/O registers

The following table lists all the XGA indexed access I/O registers. Where a G191 address is given, the register does not reside in the IMS G200, but resides in the IMS G191. The IMS G200 delivers an address to the IMS G191 to access the register. Where no G191 address is given the register resides in the IMS G200.

There are four registers which are shared by the IMS G200 and the IMS G191 (index 30, 50, 51 and 54). These registers reside in both chips.

G200 Index	G191 Addr.	Register		Read/ Write	Description
00 01 02		Memory configuration 0 Memory configuration 1 Memory configuration 2			These registers are card design specific and are used to configure the chip. They will vary depending on the amount and type of VRAM used. See Section 21.7.3 below for a description of each register.
03					RESERVED
04		Auto-configuration		Read	Indicates whether the subsystem is interfaced to a 16 or a 32 bit system interface.
05-0B					RESERVED
0C 0D		Coprocessor save/restore	data a data B		These registers are an image of a port in the coprocessor. They are used to save and restore the two parts, A and B, of the internal state of the coprocessor.
0E-0F					RESERVED
10 11		Horizontal total	Lo Hi	R/W	These registers define the total length of a scan line in units of eight pixels.
12 13		Horizontal display end	Lo Hi	R/W	These registers define the position of the end of the active picture area relative to (after) the start of the active picture area in units of eight pixels.
14 15		Horizontal blanking start	Lo Hi	R/W	These registers define the position of the end of the picture border area relative to (after) the start of the active picture area in units of eight pixels.
16 17		Horizontal blanking end	Lo Hi	R/W	These registers define the position of the start of the picture border area relative to (after) the start of the active picture area in units of eight pixels.
18 19		Horizontal sync pulse start	Lo Hi	R/W	These registers define the position of the start of horizontal sync pulse relative to (after) the start of the active picture area in units of eight pixels.
1A 1B		Horizontal sync pulse end	Lo Hi	R/W	These registers define the position of the end of horizontal sync pulse relative to (after) the start of the active picture area in units of eight pixels. This Extended Graphics Mode register is also used in 132 Column Text Mode in place of the VGA 'End Horizontal Retrace' register. In that mode each eight pixel unit is equivalent to one character.

G200 Index	G191 Addr.	Register		Read/ Write	Description
1C 1E		Horizontal sync position		Write	These registers allow the HSYNC signal to be delayed by up to 6 pixels. The required value **must** be written to both registers. Note that for a delay of four pixels this value is zero.
1D					RESERVED
1F					RESERVED
20 21		Vertical total	Lo Hi	R/W	These registers define the total length of a **frame** in units of one scan line.
22 23		Vertical display end enable	Lo Hi	R/W	These registers define the position of the end of the active picture area relative to (after) the start of the active picture area in one scan line units.
24 25		Vertical blanking start	Lo Hi	R/W	These registers define the position of the end of the picture border area relative to (after) the start of the active picture area in units of one scan line.
26 27		Vertical blanking end	Lo Hi	R/W	These registers define the position of the start of the picture border area relative to (after) the start of the active picture area in units of one scan line.
28 29		Vertical sync pulse start	Lo Hi	R/W	These registers define the position of the start of the vertical sync pulse relative to (after) the start of the active picture area in units of one scan line.
2A		Vertical sync pulse end		R/W	This register defines the position of the end of vertical sync pulse. The value loaded is the Least Significant (LS) byte of a 16 bit value which defines the end of the vertical sync pulse relative to (after) the start of the active picture area in units of one scan line. The vertical sync end position **must** be within 31 scan lines of the vertical sync start position.
2B					RESERVED
2C 2D		Vertical line compare	Lo Hi	R/W	These registers define the position of the end of the scrollable picture area relative to (after) the start of the active picture area in units of one scan line.
2E-2F					RESERVED
30* 31	03	Sprite horizontal start	Lo Hi	R/W	These registers define the position of the start of the Sprite relative to (after) the start of the active picture area in pixels.
32	04	Sprite horizontal preset		R/W	This register defines the horizontal position within the 64 by 64 sprite area at which the sprite starts. The sprite always ends at position 63 (i.e. it does not wrap).

G200 Index	G191 Addr.	Register		Read/ Write	Description
33 34		Sprite vertical start	Lo Hi	R/W	These registers define the position of the start of the Sprite relative to (after) the start of the active picture area in units of one scan line.
35		Sprite vertical preset		R/W	This register defines the vertical position within the 64 by 64 sprite area at which the Sprite starts. The sprite always ends at position 63 (i.e. it does not wrap).
36	05	Sprite control		R/W	This register controls whether the Sprite is visible or invisible.
37					RESERVED
38 39 3A 3B 3C 3D	38 39 3A 3B 3C 3D	Sprite color 0 red Sprite color 0 green Sprite color 0 blue Sprite color 1 red Sprite color 1 green Sprite color 1 blue		R/W	These registers define the red, green and blue components of the pixels displayed when the sprite data for those pixels selects Color 0 or Color 1.
3E-3F					RESERVED
40 41 42		Display pixel map offset	Lo Mi Hi	R/W	These registers define the address of the start of the visible portion of the video buffer in units of 8 bytes.
43 44		Display pixel map width	Lo Hi	R/W	These registers define the width of the Display Pixel Map in units of 8 bytes.
45-4F					RESERVED
50*	06	Display control 1		R/W	This register contains fields defining the display blanking, display scan order, video extension enabled/disabled, and sync polarity.
51*	07	Display control 2		R/W	This register contains fields defining the pixel size (for the serializer, palette and DAC) and the display scale factors (horizontal and vertical).
52	08	Display ID and comparator		Read	This register contains fields indicating the type of display attached and the state of three diagnostic status bits associated with the DAC.
53					RESERVED
54*	0A	Clock frequency select 1		R/W	Selects the IMS G191 clock scale factor and the register used to program the pixel clock.
55	0B	Border color		R/W	This register holds the Border Color palette index.
56*	0C	Fixed clock frequency address		R/W	Used to address the Fixed pixel clock frequency registers.
57*	0D	Fixed clock frequency data		R/W	Provides access to the Fixed pixel clock frequency registers.
58*	0E	Programmed pixel clock frequency		R/W	Can be programmed to contain a frequency value for the IMS G191 PLL.
59-5A					RESERVED
5B*	1D	Miscellaneous control 1			Controls a number of IMS G191 functions.

G200 Index	G191 Addr.	Register	Read/ Write	Description
5C-5F				RESERVED
60 61	10 11	Sprite/palette index Lo Sprite index Hi	R/W	These registers are used for specifying the index when reading from the Sprite or the Palette, with subsequent incrementing of the index.
62 63	12 13	Sprite/palette index with prefetch Lo Sprite index with prefetch Hi	R/W	These registers are used for specifying the index when reading from the Sprite or the Palette.
64	14	Palette mask	R/W	The contents of this register are ANDed with each Display Memory Pixel Value and the result is used to index the palette.
65	15	Palette data	R/W	This register contains an image of the currently selected Palette RAM location.
66	16	Palette sequence	R/W	This register contains two fields, one defining which of the R,G or B elements of the currently selected palette location is the current one for the Palette data register, the other defining the sequence to be followed for selecting the R,G and B elements for successive Palette Data Register accesses.
67 68 69	17 18 19	Palette red prefetch Palette green prefetch Palette blue prefetch	R/W	These registers are not used for any normal function but **must** be saved and subsequently restored by any interrupting code that uses the sprite or palette registers.
6A	1A	Sprite data	R/W	This register is an image of the currently selected Sprite buffer location.
6B	1B	Sprite prefetch register	R/W	This register is not used for any normal function but **must** be saved and subsequently restored by any interrupting code that uses the sprite or palette registers.
6C*	1E	Miscellaneous control 2		Controls blanking of red and blue DACs.
6D-6F				RESERVED
70*	37	Clock frequency select 2	R/W	Used in conjunction with the Clock frequency select 1 register.
71-7F				RESERVED

Note: A * denotes that this register is shared by the IMS G200 and IMS G191.

Table 21.5 Indexed I/O register descriptions

21.7.3 IMS G200 memory configuration registers

The memory configuration registers (index 00, 01 and 02) should not be used or relied upon in any application software. They are card design specific and are used to configure the chip and will vary depending on the amount and type of VRAM used.

All bits marked '–' are reserved and must be masked out on reads and written to 0 (low) on writes unless otherwise specified.

Memory configuration 0 register (Index: 00)

The memory configuration register 0 sets the video memory port width.

7	6	5	4	3	2	1	0
–	–	–	–	–	–	PW	

PW (bits 0:1)	00	RESERVED
	01	16 bit serial data width
	10	32 bit serial data width
	11	RESERVED

Memory configuration 1 register (Index: 01)

The memory configuration register 1 sets the position of the RAS and CAS strobes to the VRAM.

7	6	5	4	3	2	1	0
–	–	–	–	–	RA	RP	VA

Bit name	Definition
VA	When set to 1 it extends CAS and RAS active time for VRAM cycles, except refresh cycles.
RP	When set to 1 it extends RAS precharge time between consecutive VRAM cycles.
RA	When set to 1 it extends CAS and RAS active time for VRAM refresh cycles.

Memory configuration 2 register (Index: 02)

7	6	5	4	3	2	1	0
–	–	–	–	MT	–	–	–

MT	0	VRAM serializer length = 256
	1	VRAM serializer length = 512

21.7.4 IMS G200 VGA indexed access I/O registers

The IMS G200 contains all the VGA registers (as defined in the 'Video subsystem' section in the *IBM Video Technical Reference*, document number 42G2193), with the exception of those registers or register bits listed below which are in the IMS G191. For a complete list of those VGA registers which reside in the IMS G191 refer to the *IMS G191 XGA serializer palette DAC datasheet*, document number 42 1550 02.

VGA Address		IMS G191 VGA Index	Bits not in IMS G200	Register name
Wr @	Rd @			
3C0	3C1	N/A	5	Attribute address
3C0	3C1	3C0=0-0F	All bits	Internal palette
3C0	3C1	3C0=10	All bits	Attribute mode control
3C0	3C1	3C0=11	All bits	Attribute overscan color
3C0	3C1	3C0=12	All bits	Attribute color plane enable
3C0	3C1	3C0=13	All bits	Attribute horizontal pixel pan
3C0	3C1	3C0=14	All bits	Attribute color select
3C2	3CC	N/A	2,3	Miscellaneous output
N/A	3C2	N/A	4	Input status zero
3C5	3C5	3C4=00	All bits	Sequencer reset
3C5	3C5	3C4=01	All bits	Sequencer clocking mode
3CF	3CF	3CE=05	5,6	Graphics mode
3C6	3C6	N/A	All bits	Palette mask
3C7	3C7	N/A	All bits	Palette pixel address (Rd)/ DAC state
3C8	3C8	N/A	All bits	Palette pixel address (Wr)
3C9	3C9	N/A	All bits	Palette data

Note: 'All bits' refers to all bits defined in the *IBM PS/2 Hardware Interface Technical Reference*

21.7.5 IMS G200 XGA POS registers

The following section describes the Programmable Option Select (POS) registers which are on the IMS G200.

These registers are accessible when a SETUP cycle is performed. Setup cycles occur when the **notSetup** pin on the IMS G200 is active during the access.

POS Register 0: (notSetup and Address0-2 ='000'b)

Identification Low Byte. Read only.

Returns 'DB' hex for XGA.

POS Register 1: (notSetup and Address0-2 ='001'b)

Identification High Byte. Read only.

Returns '8F' hex.

POS Register 2: (notSetup and Address0-2= '010'b)

7	6	5	4	3	2	1	0
External Memory Addr				IODA			EN

Bit name	Definition
XGA Enable (EN)	When set to 1 identifies that the subsystem is enabled for address decoding for all non POS addresses. When 0, only POS registers can be accessed, all other accesses to the subsystem have no effect.
I/O Device Address (IODA)	This field specifies which set of I/O addresses has been allocated to the IMS G200 registers, i.e. the instance number (refer to Figure 21.6, page 414).
External Memory Address	This field specifies which of sixteen possible 8 Kbytes memory locations has been assigned to the XGA external memory. The external memory occupies the first 7 Kbytes of this 8 Kbytes block, the other 1 Kbyte being occupied by the coprocessor memory-mapped registers (see Figure 21.7, page 415).

POS Register 3: (notSetup and Address0-2= '011'b)

7	6	5	4	3	2	1	0
0	Arbitration Level				FE	EM	0

Bits 0 and 7 must be written to 0 for normal use.

Bit name	Definition
EM	External Memory Enable 0 = External Memory Address Decoding Disabled. (See POS Register 2 bits 4-7) 1 = External Memory Address Decoding Enabled. (See POS Register 2 bits 4-7)
FE	Fairness Enable 0 = Micro Channel Fairness Protocol Disabled. 1 = Micro Channel Fairness Protocol Enabled.
Arbitration Level	This 4 bit field is loaded with the 4 bit priority level to be used during Bus Master arbitration.

POS Register 4: (notSetup and Address0-2= '100'b)

7	6	5	4	3	2	1	0
Video Memory Base							VE

Bit name	Definition
Video Memory Base Address	This register contains the most significant 7 bits of the address at which the XGA external memory is located. Three more bits are provided by the I/O Device Address in POS byte 1. This gives a Video Memory Base address on a 4Mbyte boundary.
Video Memory Enable (VE)	This bit signifies whether the 4Mbyte Aperture is available for use. When this bit is set to 0 the 4Mbyte Aperture is disabled, and when set to 1 the 4Mbyte Aperture is enabled.

POS Register 5: (notSetup and Address0-2 ='101'b)

7	6	5	4	3	2	1	0
1	1	0	1	1Mbyte Base			

Bit name	Definition
1Mbyte Base	This field specifies where the 1Mbyte Aperture has been positioned in system address space in increments of Mbytes. A 0 in the field will disable the aperture.

21.8 IMS G200 / IMS G191 communication

21.8.1 IMS G191 register accesses

Because the Micro Channel bus interface function is implemented by the IMS G200 display controller, all updates to registers physically resident in the IMS G191 are decoded by the IMS G200 which then updates the IMS G191. Data for these registers is transferred over the **Data0-7** pins; the address being generated by the IMS G200 **VAddr0-6** pins driving IMS G191 **RegAddr0-6**.

Parameter register accesses are timed by the IMS G200 controller clock (**Clk**), which results in a clock period of 50ns (with the controller operating at 40MHz). A parameter register access occurs whenever **notDataStrobe** is active and address bit 6 is '0'.

There are two basic types of accesses between the IMS G200 and IMS G191, fast accesses and slow accesses. Fast accesses are used for parameter register updates to the IMS G191 and slow accesses are used for sprite/palette accesses since extra time is needed to allow the sprite buffer or the palette RAM to be accessed.

21.8.2 Control codes from the IMS G200 to the IMS G191

The address bits on the IMS G200/IMS G191 interface are used at certain times to carry control data from the IMS G200 to the IMS G191. This data is not transferred as a result of Micro Channel activity, but during each VRAM transfer cycle, in particular during the transfer cycle at the start of each line. This data mainly consists of information about the line that is about to be displayed. The data is not transferred on the data bus, but on the low-order six bits of the address.

These bits are encoded as shown in Table 21.6 with their usage described in Table 21.7.

RegAddr0-6							IMS G191 decoded meaning
6	5	4	3	2	1	0	
0	@	@	@	@	@	@	IMS G191 parameter register address
1	0	N	A	S	U	C	control code
1	1	R	R	R	R	R	control code

Table 21.6 Encoding of register address bits 0-6

Symbol	Register address bit usage
@	Address bits used to address the parameter registers within the IMS G191
N	The 'new font pair' bit. When this bit is '1' it causes a reset of the sprite buffer address register used during alphanumeric font loading.
A	The 'active line' bit. This bit is '1' for picture lines, and '0' for border (overscan) lines and for blank (flyback) lines.
S	The 'scrollable/border line' bit. When it is '1' during an active line it indicates that the line is scrollable. When it is '1' during a non-active line it indicates that the line is a border line.
U	The 'underline/panning sync/sprite line' bit. In an alphanumeric VGA mode it is '1' to indicate that the underline part of a character should be placed on the line. In extended mode it is '1' to indicate that the sprite should be placed on the line. In addition, if this bit is '1' during a non-active line, it causes the horizontal panning sync register to be strobed.
R	In VGA mode these bits are character row bits 4:0. In extended mode these bits hold the sprite prefetch row number, indicating in which row the sprite is to be displayed.
C	C is bit 5 of the sprite row number.

Table 21.7 Register address bit usage

21.8.3 Video control

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G200 from the IMS G191 CRTC clocks and fed back into the IMS G191 via the **VideoCtrlIn0-1** pins. The video control signals are encoded as shown in Table 21.8 to indicate events on a horizontal scan line.

VideoCtrlOut0-1		Video data function
Bit 1	Bit 0	
0	0	Blanking
0	1	Border
1	0	Picture
1	1	Picture and start of cursor

Table 21.8 **VideoCtrlOut0-1** decoding

21.9 Hardware interfaces

The IMS G200 display controller interfaces to several other components in an XGA subsystem. These include the the Micro Channel system bus, IMS G191 serializer palette DAC, VRAM, ROM and external registers.

21.9.1 System bus interface

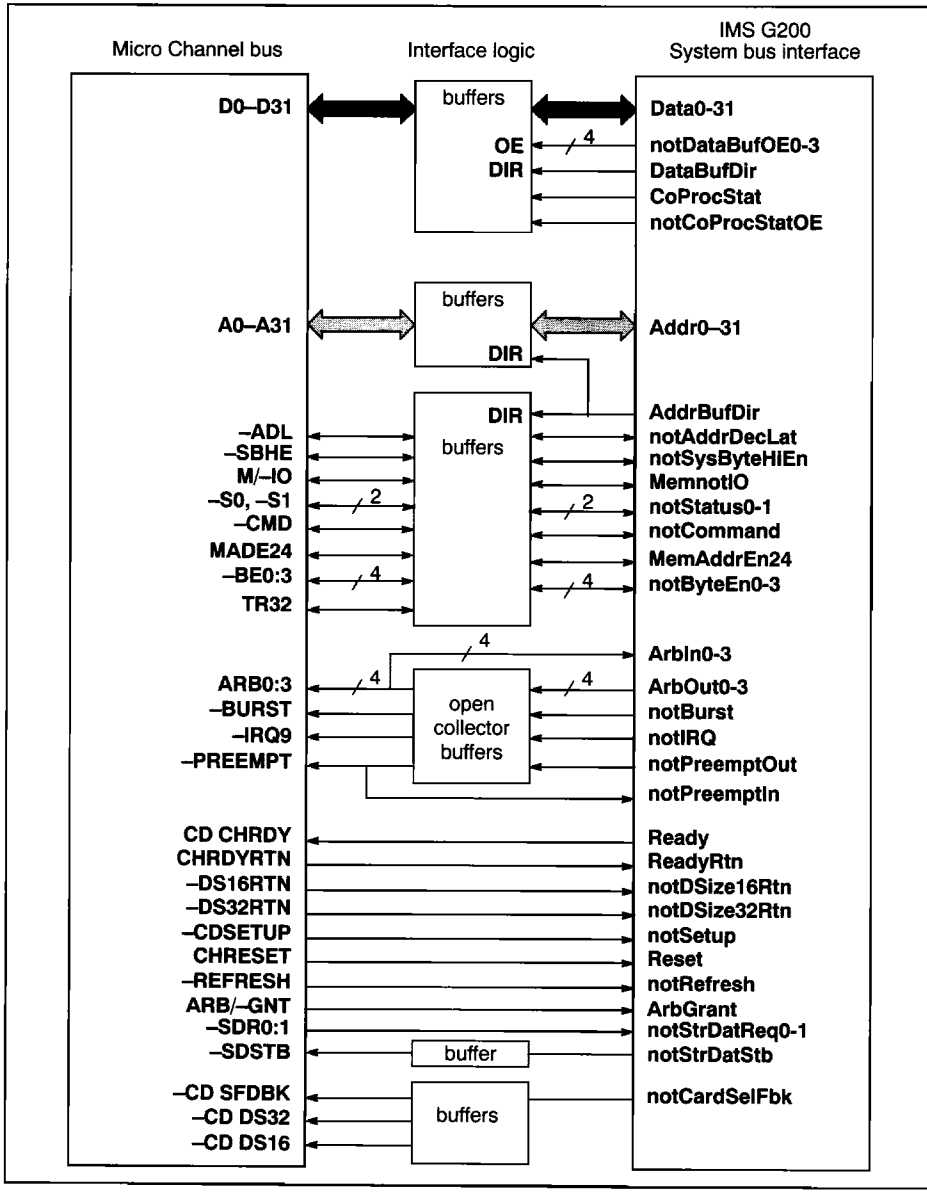


Figure 21.8 IMS G200 system bus interface

The system bus interface consists of the address, data, and controls defined in the Micro Channel specification. When the coprocessor is being used in system memory, bus mastership is utilized. A bus master controls the bus and supplies addresses for the bus cycles. Either 16 or 32 bit channels are supported. Figure 21.8 shows the IMS G200 signals used to interface with the Micro Channel bus.

The IMS G200 can act either as Master or Slave with either a 16 or 32-bit interface depending on the card configuration. Micro Channel streaming data operation is supported when the IMS G200 is bus master only.

The Micro Channel architecture defines an arbitration procedure through which all prospective bus masters go. The outcome of this arbitration procedure is that one card is granted bus mastership status. This card then controls all cycles on the bus, providing addresses for each cycle or burst of cycles until another card becomes the bus master.

Provision is made within the Micro Channel specification for a slave to extend a cycle when being asked to supply data by using the ready signal.

The IMS G200 in particular always uses this Channel Ready signal (**CD CHRDY**) in order to force an extended cycle when in slave mode.

Certain signals in the Micro Channel definition must be driven by an open collector device. The arbitration (ARB) signals are an example. The IMS G200 display controller splits these into two signals, an input (**ArbIn**) and an output (**ArbOut**). Figure 21.9 shows how a typical open collector Micro Channel signal would be buffered. The Micro Channel ARB signal is driven by a three-state buffer whose enable is driven by **ArbOut**. Refer to the IBM Micro Channel specification for further details.

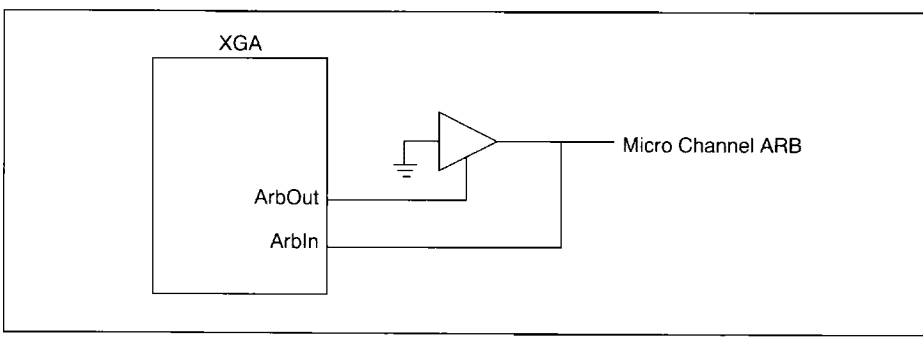


Figure 21.9 External buffer for Micro Channel signals requiring open collector drivers

21.9.2 VRAM interface

The IMS G200 display controller controls all operations to the VRAM. On the random port, refresh cycles, serializer transfer cycles, system read/write, and coprocessor read/write cycles are performed. On the serial port, the serializer shift clock is provided. The IMS G200 display controller can support VRAM widths of either 16 or 32 bits.

The data bus (**Data0-31**) is shared by the VRAM and the system bus. Isolation buffers are required to allow this dual use. The VRAM data is also used to communicate with the IMS G191 serializer palette DAC, external registers and ROM.

All control signals for the VRAM are generated in the IMS G200 display controller. This includes **notVRAS0-1**, **notVCAS0-1**, **notVOE**, **notVWE0-3** and **VSClk**.

Figure 21.10 shows the connections between the VRAM controller of the IMS G200 and the external VRAM.

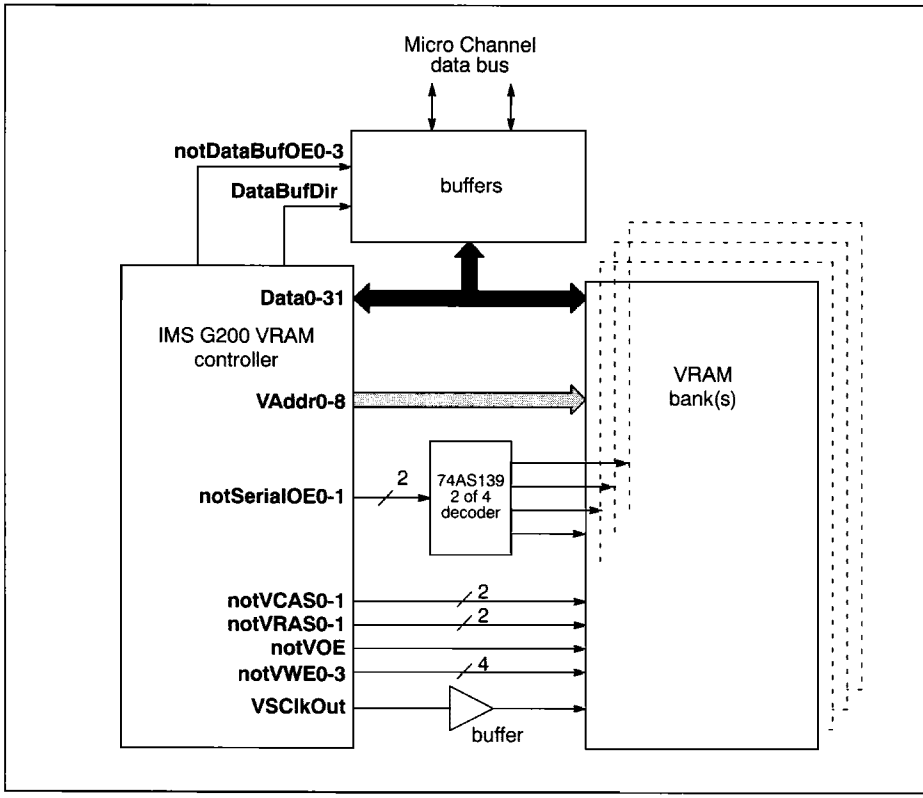


Figure 21.10 IMS G200 VRAM interconnection

VRAM Transfer Cycles

Transfer cycles are generated at the start of every line and every time the VRAM serializer becomes empty. Depending on the screen width and where the VRAM base address was assigned, two transfer cycles are generated at the start of some lines if the serializer becomes empty just after the start of a line.

Support for multiple VRAM banks

The IMS G200 now supports up to 4 MBytes of VRAM consisting of devices using nine row and nine column address lines. The VRAM internal architecture must consist of a number of 512 x 512 (256 KBytes) memory arrays, typically 256K x 4, since the IMS G200 supports a 9-bit multiplexed VRAM address bus. Care should be taken not to exceed the IMS G200 pin output loading characteristics, given in Table 21.25, when connecting multiple VRAM devices.

The IMS G200 framestore manager supports up to four banks of VRAM populating the full 32-bit data and pixel path using **notVRAS0**, **notVRAS1**, **notVCAS0** and **notVCAS1** (pins formerly assigned as **notVRAS**, **N/C**, **notVCAS** and **N/C**). The four VRAM banks are configured using these strobes as follows:

Bank 0	Bank 1	Bank 2	Bank 3
notVRAS0	notVRAS0	notVRAS1	notVRAS1
notVCAS0	notVCAS1	notVCAS0	notVCAS1

The VRAM column and row address strobes are coded as shown in Table 21.9. The column address coding allows any bank in the XGA subsystem to be uniquely accessed (**notVCAS0-1** - H, **notVRAS0-1** - H) whilst the second row addressed bank (**notVCAS0-1** - L, **notVRAS0-1** - H) is refreshed at the row address presented.

VRAM bank	notVRAS0	notVRAS1	notVCAS0	notVCAS1
0	L	H	L	H
1	L	H	H	L
2	H	L	L	H
3	H	L	H	L

Table 21.9 Coding of VRAM column and row address strobes

In addition to supporting multiple banks on the random access port the IMS G200 provides coded serial output enable strobes (**notSerialOE0-1**) to multiplex pixel data from any one of four VRAM serial ports. Typically, an external decoder with inverting outputs ($^1/_2$ of 74AC139) is used to perform the serial output enable function of the required VRAM banks as defined in Table 21.10.

notSerialOE0	notSerialOE1	Bank selected
0	0	0
0	1	1
1	1	2
1	0	3

Table 21.10 Coding of VRAM serial output enable strobes

21.9.3 IMS G191 serializer palette DAC interface.

Figure 21.11 shows the signals used within the IMS G200 to connect the IMS G191 serializer palette DAC.

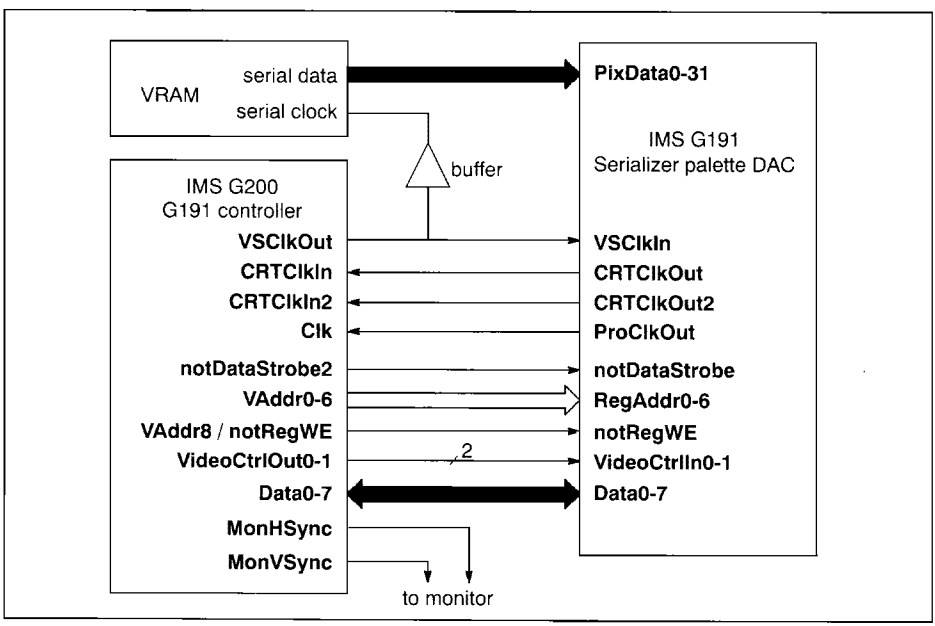


Figure 21.11 IMS G200 interface to the IMS G191

The **notDataStrobe2** output from the IMS G200 is dedicated to the IMS G191. It is used to strobe addresses and control code data (carried on the **VAddr0-6** bus) from the IMS G200 to the IMS G191. It is used to communicate register contents programmed by the host processor and decoded in the IMS G200. A low sent on this pin to the IMS G191 indicates that the IMS G191 should perform the action defined by the **VAddr0-6** and **notRegWE** pins.

The **notRegWE** pin is driven by bit 8 (**VAddr8**) of the VRAM address bus during accesses between the IMS G200 and IMS G191. It determines whether a read or write cycle is being executed. When low, indicating a write to the IMS G191, it inputs the data (**Data0-7**) into the IMS G191 addressed parameter register. When high, indicating a read from the IMS G191, it outputs the contents of the addressed parameter register onto the data bus.

The data bus (**Data0-7**) is bi-directional between the IMS G200 and the IMS G191 and transfers parameter register data.

G200 writes to G191 registers

For IMS G191 register writes, data is passed from the IMS G200 to the IMS G191 in byte-wide chunks over the data bus (**Data0-7**). All 8 bits of data are passed to the IMS G191 for shared registers, as well as for the other registers. For shared registers the IMS G200 also latches its required data at the same time.

Micro Channel Registers in the IMS G200 and the IMS G191 which have duplicate bits are written to in both chips. The slowest write controls the **Ready** signal to the Micro Channel. G200 writes to G191 registers are shown in Figure 21.12.

Write to G191 register timings

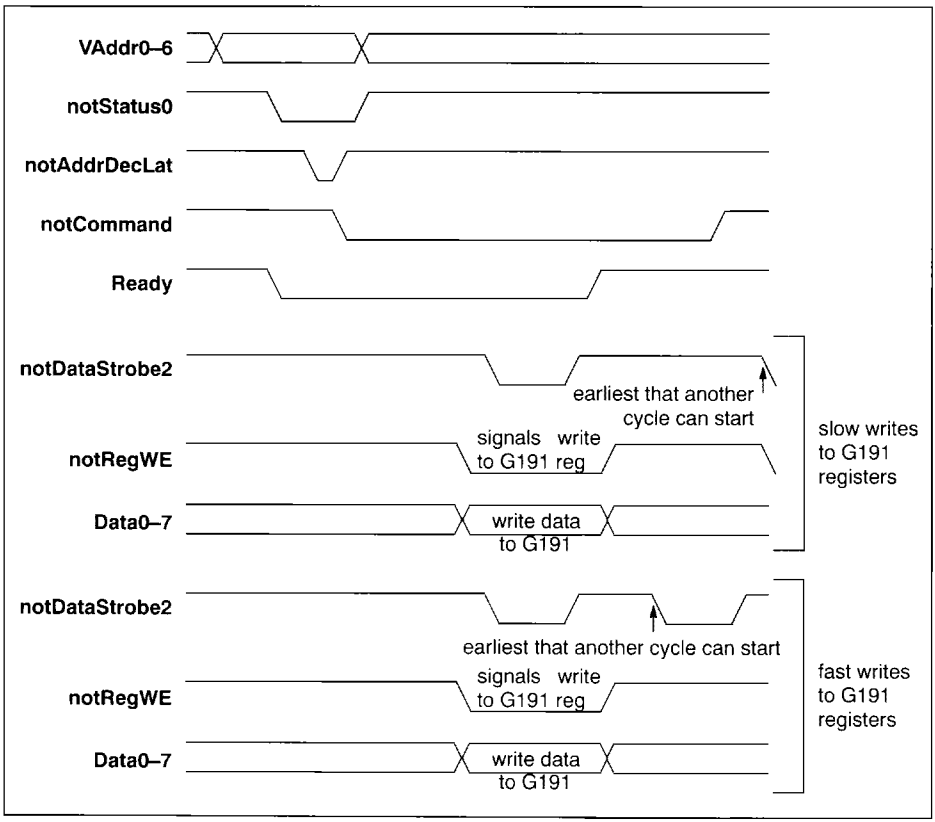


Figure 21.12 G200 writes to G191 registers

G200 reads of G191 registers

For IMS G191 register reads data is read from the IMS G191 via the data bus and latched in the IMS G200. Any shared registers are then OR'ed to ensure data consistency. Any bits which are duplicated between registers in the IMS G200 and IMS G191 are also OR'ed. The IMS G200 then performs any necessary operations on the data before passing it to the Micro Channel. G200 reads of G191 registers are shown in Figure 21.13.

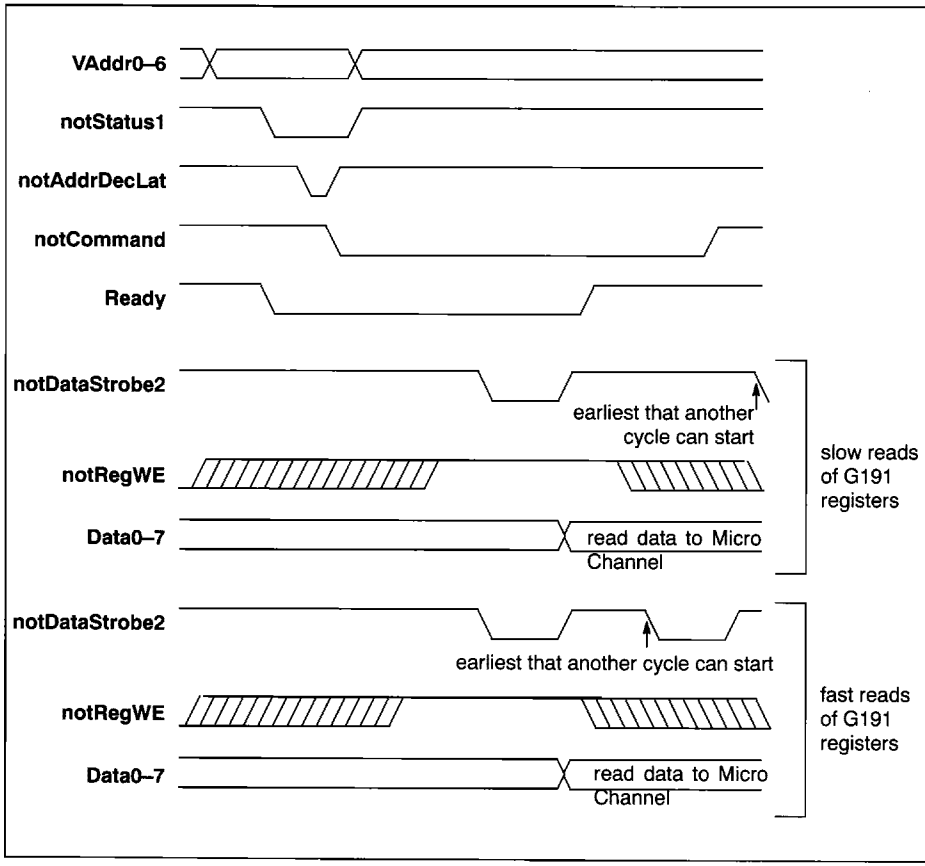


Figure 21.13 G200 reads of G191 registers

21.9.4 External memory and register interface

Reads and writes to external registers and static memory are handled in a similar way to IMS G191 register reads and writes. The **notDataStrobe1** signal strobes low to cause reads and writes to/from external memory (typically PROM) and external registers. This signal is qualified by one of the data bits (**Data28-31**) to select a particular type of operation, as follows:

Data28	External memory write
Data29	External memory read
Data30	External register write
Data31	External register read

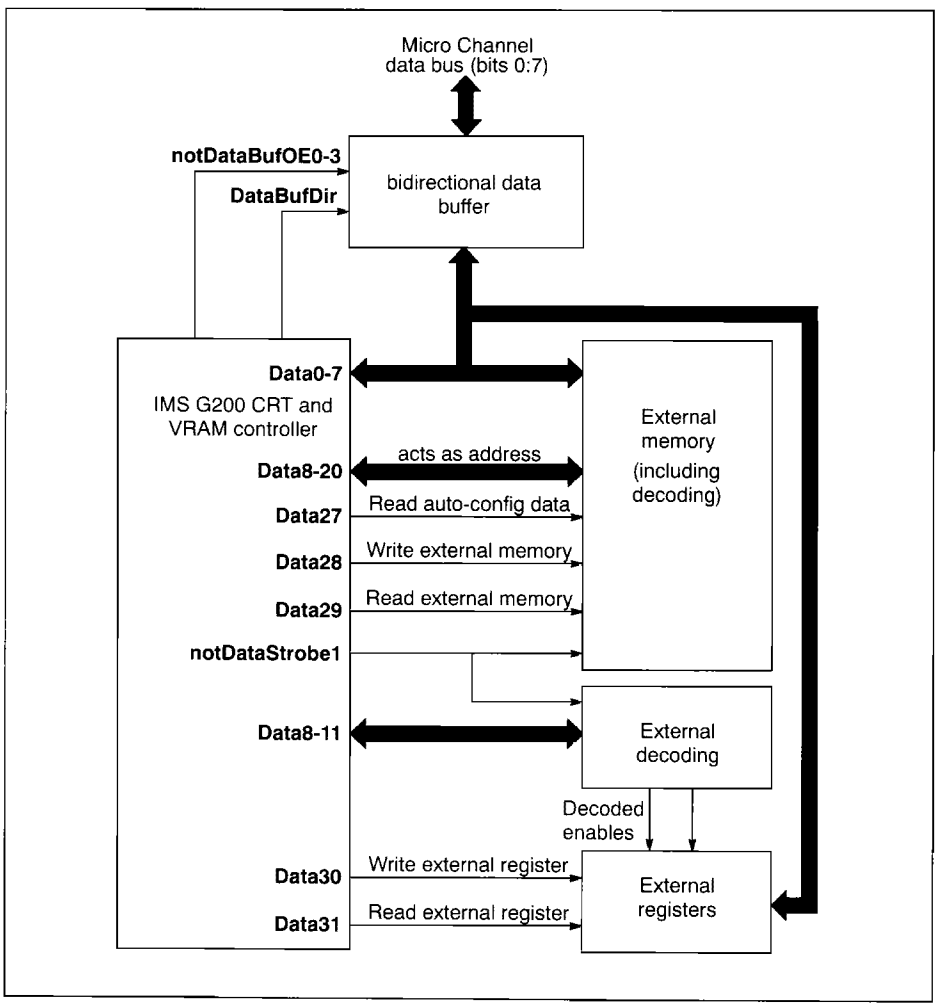


Figure 21.14 IMS G200 external memory and register interface

External memory accesses

The IMS G200 supports an external ROM or RAM device and can map it into system address space. When the external storage is accessed, the IMS G200 generates a low pulse on **notDataStrobe1**. During a read from external storage, **notDataStrobe1** will be qualified by **Data29** being low. A write will be qualified by **Data28** being low. This is the mechanism for supporting an adapter BIOS ROM. Programmable Option Select (POS) registers define the decoding range of the external storage.

The address for the external storage access is driven on **Data8-20** and data is driven on **Data0-7**.

External register accesses

Some implementations of the XGA subsystem require the use of external registers accessible by the system processor. The IMS G200 assists in this by providing a range of decodes for which a strobe signal and qualifiers are generated. External register operation is similar to external memory access. **notDataStrobe1** is the strobe pulse that is qualified by **Data30** for writes and **Data31** for reads. **Data8-11** are available for decoding specific registers, as defined below.

XGA indexed register 21xA	Data8-11 external register address	Description
70	0	External clock select register
71-7F	1-F respectively	Reserved

21.10 Reset and Initialization

On reset and during initialization the IMS G200 goes through a procedure called Auto Configuration. The auto configuration cycle is an automatic procedure which occurs during **Reset**. During this cycle **notDataStrobe1** and **Data27** will pulse low. This is the only time that both of these pins will pulse low together.

During this time the following must be ensured:

Data0 is held to 0 (low) for a 16 bit system interface, and held to 1 (high) for a 32 bit system interface.

Data1 is held to 1 (high) for proper operation.

Data2 is held to 1 (high) for proper operation.

A diagram showing reset timings is given in Figure 21.36.

21.11 Timing reference guide

21.11.1 System bus interface timings

This section provides timing diagrams for the basic I/O and memory cycles. For Figures 21.15 and 21.16 IMS G200 signal names are shown in the left-hand and Micro Channel names in the right-hand column.

I/O and memory cycle timings for IMS G200 as Micro Channel bus master

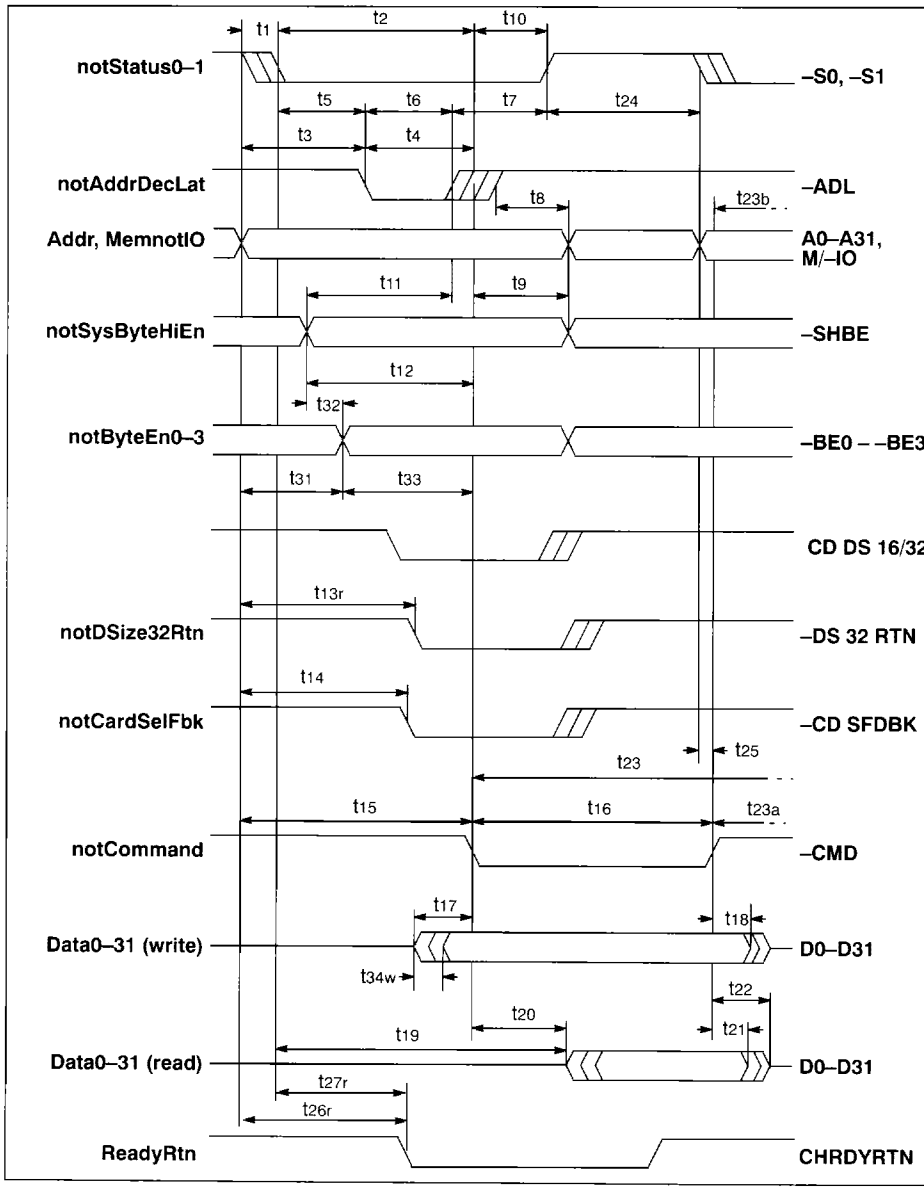


Figure 21.15 I/O and memory cycle timings for IMS G200 as bus master

Symbol	Parameter	Micro Channel		IMS G200		Units
		Min	Max	Min	Max	
t1	**notStatus0-1** active from **Addr, MemnotIO** valid	10		20		ns
t2	**notCommand** active from **notStatus0-1** active	55		65		ns
t3	**notAddrDecLat** active from **Addr, MemnotIO** valid	45		55		ns
t4	**notAddrDecLat** active to **notCommand**	40		50		ns
t5	**notAddrDecLat** active from **notStatus0-1** active	12		22		ns
t6	**notAddrDecLat** pulse width	40		45		ns
t7	**notStatus0-1** hold from **notAddrDecLat** inactive	25		35		ns
t8	**Addr, MemnotIO** hold from **notAddrDecLat inactive**	25		31		ns
t9	**Addr, MemnotIO** hold from **notCommand** active	30		36		ns
t10	**notStatus0-1** hold from **notCommand** active	30		40		ns
t11	**notSysByteHiEn** setup to **notAddrDecLat** inactive	40		50		ns
t12	**notSysByteHiEn** setup to **notCommand** active	40		50		ns
t13r	**notDSize32Rtn** valid from **Addr, MemnotIO** valid		75		88	ns
t14	**not CardSelFbk** valid from **Addr, MemnotIO** valid				*	
t15	**notCommand** active from **Addr** valid	85		95		ns
t16	**notCommand** pulse width	90		95		ns
t17	Write **Data0-31** setup to **notCommand** active	0		10		ns
t18	Write **Data0-31** hold from **notCommand** inactive	30		40		ns
t19	**notStatus0-1** to Read **notData0-31** valid		125		138	ns
t20	Read **Data0-31** from **notCommand** active		60		73	ns
t21	Read **Data0-31** hold from **notCommand** inactive	0		–10		ns
t22	Read data bus tri-state from **notCommand** inactive		40		50	ns
t23	**notCommand** active to next **notCommand** active	190		195		ns
t23a	**notCommand** inactive to next **notCommand** active	80		90		ns
t23b	**notCommand** inactive to next **notAddrDecLat** active	40		50		ns
t24	Next **notStatus0-1** active from **notStatus0-1** inactive	30		40		ns
t25	Next **notStatus0-1** active to **notCommand** inactive		20		10	ns
t26r	**ReadyRtn** inactive from **Addr, MemnotIO** valid		80		90	ns
t27r	**ReadyRtn** inactive from **notStatus0-1** valid and previous **notCommand** inactive	0	50	–10	60	ns
t31	**notByteEn0-3** active from **Addr**		40		30	ns
t32	**notByteEn0-3** active from **notSysByteHiEn**, A0, A1 active		30		20	ns
t33	**notByteEn0-3** active to **notCommand** active	10		20		ns
t34w	Write **Data0-31** setup to write **Data0-31** hold	0	15		*	

*This is a Micro Channel system timing, for details refer to the Micro Channel specification

Table 21.11 I/O and memory cycle timings for IMS G200 as bus master

I/O and memory cycle timings for IMS G200 as Micro Channel bus slave

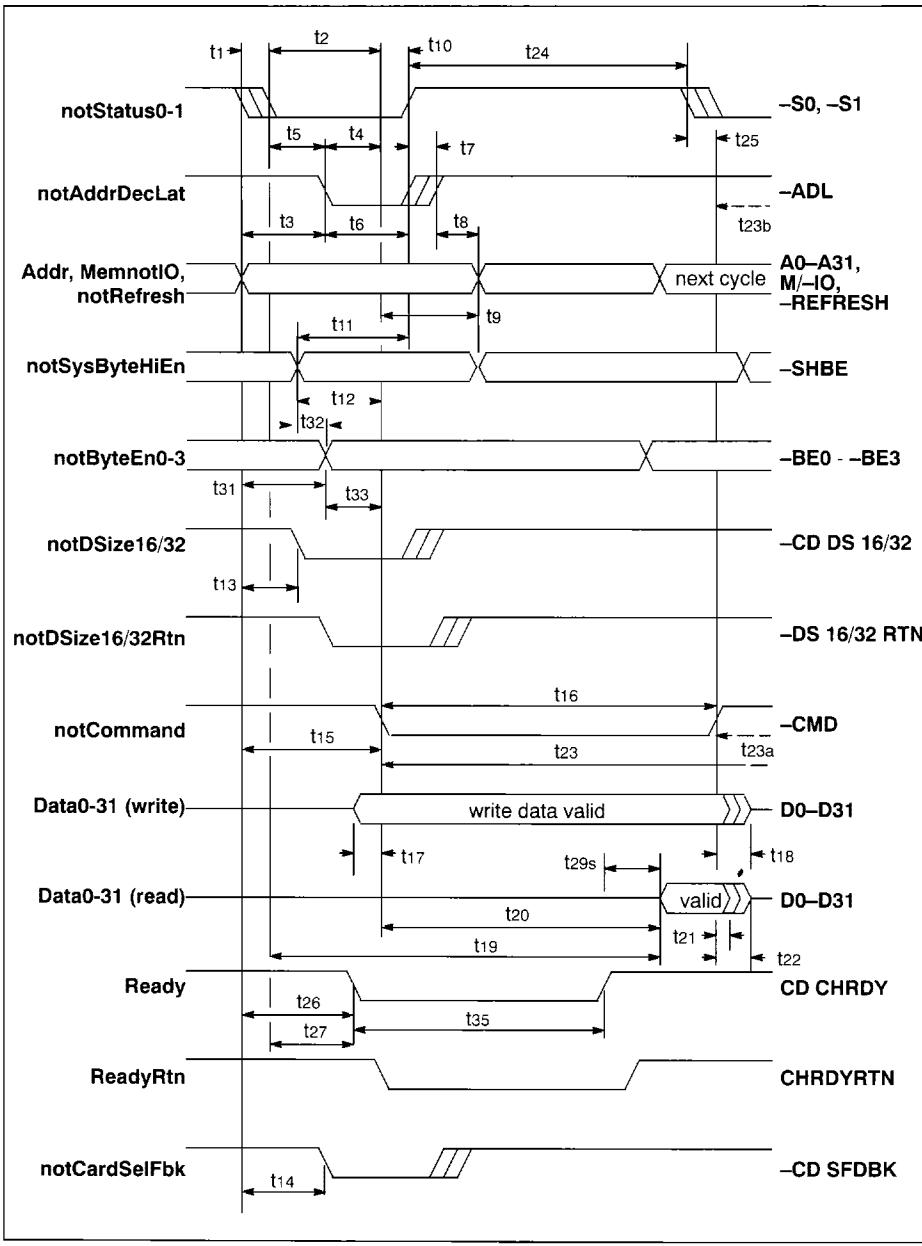


Figure 21.16 I/O and memory cycle for IMS G200 as bus slave

Symbol	Parameter	Micro Channel		IMS G200		Units	Notes
		Min	Max	Min	Max		
t1	**notStatus0-1** active from **Addr,MemnotIO, notRefresh** valid	10		0		ns	
t2	**notCommand** active from **notStatus0-1** active	55		45		ns	
t3	**notAddrDecLat** active from **Addr, MemnotIO, notRefresh** valid	45		35		ns	
t4	**notAddrDecLat** active to **notCommand**	40		30		ns	
t5	**notAddrDecLat** active from **notStatus0-1** active	12		2		ns	
t6	**notAddrDecLat** pulse width	40		30		ns	
t7	**notStatus0-1** hold from **notAddrDecLat** inactive	25		15		ns	1
t8	**Addr,MemnotIO, notRefresh, notSysByteHiEn** hold from **notAddrDecLat** inactive	25		15		ns	
t9	**Addr,MemnotIO, notRefresh, notSysByteHiEn** hold from **notCommand** active	30		20		ns	
t10	**notStatus0-1** hold from **notCommand** active	30		20		ns	1
t11	**notSysByteHiEn** setup to **notAddrDecLat** inactive	40		30		ns	
t12	**notSysByteHiEn** to **notCommand** active	40		30		ns	
t13	**notDsize16/32** valid from **Addr,MemnotIO** valid		55		42	ns	
t14	**notCardSelFbk** valid from **Addr,MemnotIO** valid		60		42	ns	
t15	**notCommand** active from **Addr** valid	85		75		ns	
t16	**notCommand** pulse width	190				ns	2
t17	Write **Data0-31** setup to **notCommand** active	0		–10		ns	
t18	Write **Data0-31** hold from **notCommand** inactive	30		20		ns	
t19	**notStatus0-1** to Read **Data0-31** valid		125		115	ns	
t20	Read **Data0-31** valid from **notCommand** active		60			ns	
t21	Read **Data0-31** hold from **notCommand** inactive	0		10		ns	
t22	Read **Data0-31** bus tri-state from **notCommand** inactive		40		30	ns	
t23	**notCommand** active to next **notCommand** active	190				ns	
t23a	**notCommand** inactive to next **notCommand** active	80		70		ns	
t23b	**notCommand** inactive to next **notAddrDecLat** active	40		30		ns	
t24	Next **notStatus0-1** active from **notStatus0-1** inactive	30		20		ns	
t25	Next **notStatus0-1** active to **notCommand** inactive		20		30	ns	
t26	**CD CHRDY** valid from **Addr** valid		60		53	ns	
t27	**CD CHRDY** valid from **notStatus0-1** valid		30		23	ns	
t29s	Read **Data0-31** valid from **Ready**		60		50	ns	
t31	**notByteEn0-3** active from **Addr** valid (32 bit masters only)		40		50	ns	
t32	**notByteEn0-3** active from **notSysByteHiEn, A0, A1** active		30		40	ns	
t33	**notByteEn0-3** active to **notCommand** active	10		0		ns	
t35	**CD CHRDY** valid from **-CD CHRDY**		3.5		3.5	µs	

Notes:

1 A bus master must deactivate **–S0,1** as soon as possible after the hold time specified by t7 and t10, and prior to the deactivation of **–CMD**. This deactivation must be independent of **CHRDYRTN**.

2 All slave cycles are extended except for accesses to the Auxiliary Coprocessor Control register. These are default cycles (**–CMD** pulse width is 90ns min).

Table 21.12 I/O and memory cycle for IMS G200 as bus slave

IMS G200 Micro Channel buffer timings in slave mode

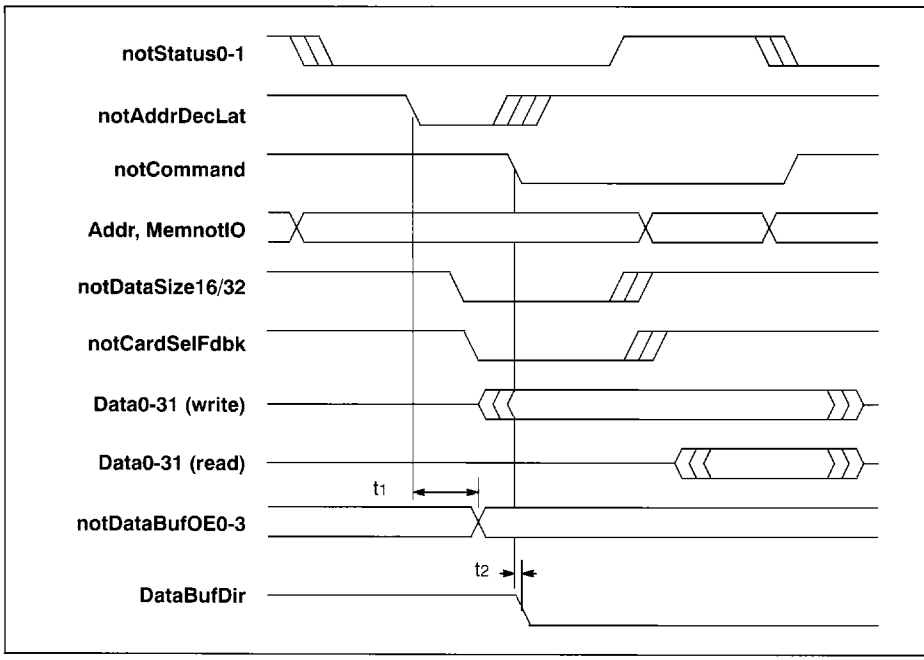


Figure 21.17 IMS G200 Micro Channel buffer timings in slave mode

Symbol	Parameter	Min	Max	Unit	Notes
t1	**AddrDecLat** to **notDataBufOE0-3** change	7	29	ns	
t2	**Command** to **DataBufDir** change	5	18	ns	

Table 21.13 IMS G200 Micro Channel buffer timings in slave mode

Timings for Micro Channel arbitration cycle

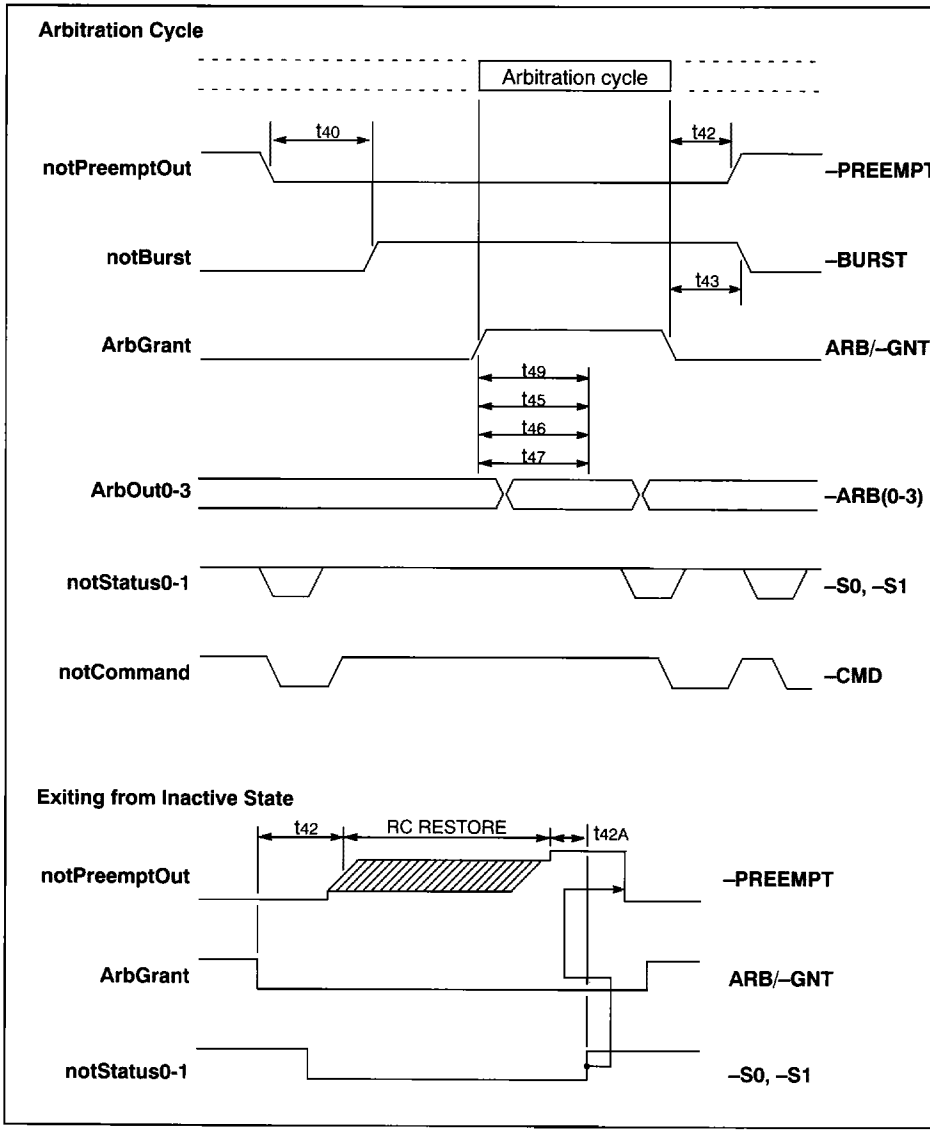


Figure 21.18 Arbitration cycle

Symbol	Parameter	Micro Channel		IMS G200		Units	Notes
		Min	Max	Min	Max		
t_{40}	**notPreempt** active (low) to end of transfer	0	7.8	0	7.5	µs	
t_{42}	**notPreempt** inactive (high) from **ArbGrant** low	0	50	0	40	ns	
t_{42A}	**notPreempt** inactive (high) to Status inactive	20		30		ns	1
t_{43}	**notBurst** active (low) from **ArbGrant** low (by bursting DMA slave)		50		40	ns	
t_{45}	Driver turn-on delay from **ArbGrant** high	0	50	0	40	ns	
t_{45A}	Driver turn-on delay from lower priority line	0	50	0	40	ns	
t_{46}	Driver turn-off delay from **ArbGrant** high	0	50	0	40	ns	
t_{47}	Driver turn-off delay from lower priority line	0	50	0	40	ns	
t_{49}	Tri-state drivers from **ArbGrant** high		50		40	ns	

Note:

1 t_{42A} represents the timing requirement after the resistor-capacitor line delay. This window is available for devices to detect inactive **–PREEMPT** and exit from the inactive state after the rising edge of **–S0, S1**.

Table 21.14 Arbitration cycle timings

Timings for Micro Channel streaming data mode

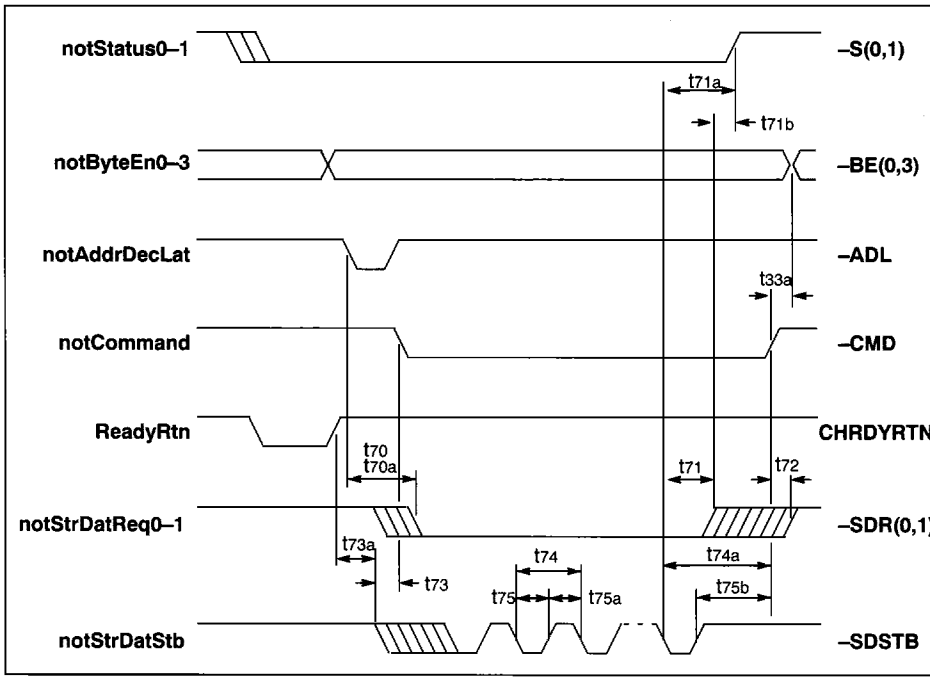


Figure 21.19 Streaming mode timing diagram for streaming data cycle basic signal sequence

Symbol	Parameter	Micro Channel		IMS G200		Units
		Min	Max	Min	Max	
t33a	**notByteEn0-3** hold from **notCommand** inactive	10		20		ns
t70	**notStrDatReq0–1** valid from **notAddrDecLat** active (slave)	0	40	–10	50	ns
t70a	**notStrDatReq0–1** valid from **notAddrDecLat** active (master)	0	115	–10	125	ns
t71	**notStrDatReq0–1** inactive from last **notStrDatStb** fall	0	40	–10	50	ns
t71a	**notStatus0-1** inactive from last **notStrDatStb** fall		10		10	ns
t71b	**notStrDatReq0–1** inactive from **notStatus0-1** inactive	0	40	–10	50	ns
t72	**notStrDatReq0–1** tristate from **notCommand** inactive	0	40	–10	50	ns
t73	**notStrDatStb** active to **notCommand** active		10		0	ns
t73a	**notStrDatStb** active from **ReadyRtn** active	0		10		ns
t74	**notStrDatStb** period	100		100		ns
t74a	**notCommand** inactive from last **notStrDatStb** fall	100		110		ns
t75	**notStrDatStb** active	35		40		ns
t75a	**notStrDatStb** inactive	35		40		ns
t75b	**notStrDatStb** inactive to **notCommand** inactive	35		45		ns

Table 21.15 Streaming mode timings for streaming data cycle basic signal sequence

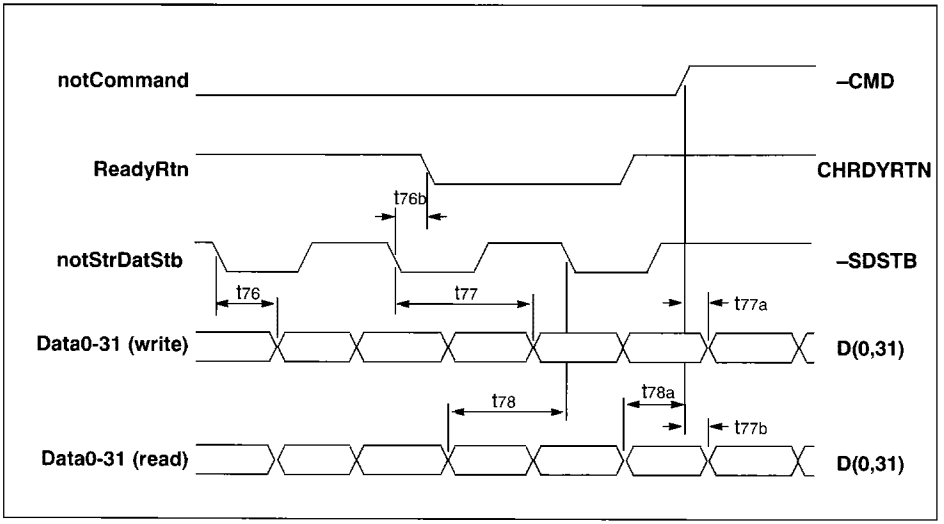


Figure 21.20 Streaming mode timing diagram for streaming data clocking

Symbol	Parameter	Micro Channel		IMS G200		Units
		Min	Max	Min	Max	
t76	**Data0-31** (send) valid from **notStrDatStb** fall		60		50	ns
t76b	**ReadyRtn** valid from **notStrDatStb** fall	3	45	–2	50	ns
t77	**Data0-31** (send) hold from **notStrDatStb** fall	10		20		ns
t77a	**Data0-31** (write) hold from **notCommand** inactive	11		21		ns
t77b	**Data0-31** (read) hold from **notCommand** inactive	7		0		ns
t78	**Data0-31** (receive) valid before **notStrDatStb** fall	25		20		ns
t78a	**Data0-31** (receive) valid before **notCommand** inactive	25		20		ns

Table 21.16 Streaming mode timings for streaming data clocking

21.11.2 VRAM interface timings

VRAM Read/Write Timings

All accesses to the random read/write port of the VRAMs are synchronous to the IMS G200 processor clock (**Clk**). The timings of these strobes vary continuously depending on the contents of memory configuration register 1.

Figure 21.21 shows a basic read and write cycle to the VRAMs. Read data from the VRAM is latched into the IMS G200 using either **notVCAS0-1** or **notVOE**, whichever becomes inactive first. This varies depending on the memory parameters, see Table 21.17.

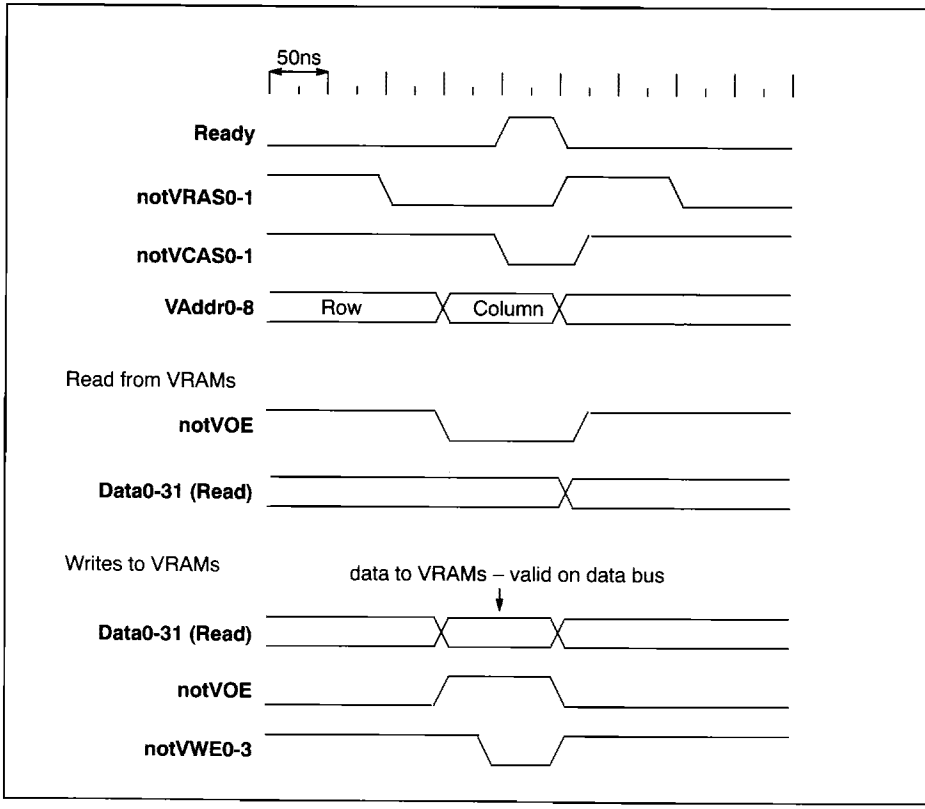


Figure 21.21 Basic memory controller access to VRAMs

Figure 21.22 shows the timings for basic multicycle accesses, alternatively referred to as page mode accesses.

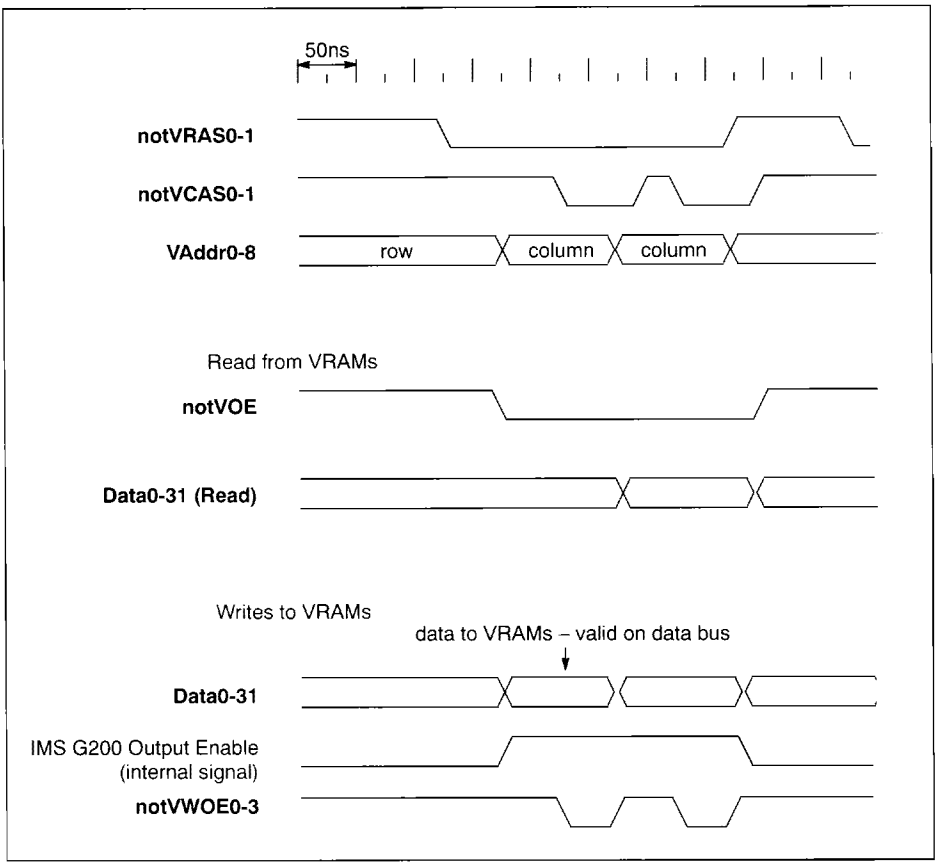


Figure 21.22 Memory controller access to VRAMs-multi cycle

Effects of setting the IMS G200 memory configuration registers

The timings of the VRAM cycles under various modes is dependent on the settings of the memory configuration register (index 01).

All bits marked '–' are reserved and must be masked out on reads and written to 0 (low) on writes unless otherwise specified.

Memory configuration 1 register (Index: 01)

7	6	5	4	3	2	1	0
–	–	–	–	–	RA	RP	VA

The previous two timing diagrams, Figures 21.21 and 21.22, showed the default timing with RA, RP and VA set to 0. Setting these bits to a value other than 0 will extend the VRAM cycles as indicated in the following table and timing diagrams.

Bit name	Bit	Definition
VA	0	When set to 1 it extends CAS and RAS active time for VRAM cycles, except refresh cycles. This parameter determines the nominal time from CAS falling to the next CAS falling during page cycles. Nominal CAS times are given below: When VA set to 0: CAS low time = 62.5ns CAS high time = 37.5ns CAS falling to CAS falling = 100ns Refresh falling to CAS falling lowtime = 112.5ns or 162.5ns When VA set to 1: CAS low time = 100ns CAS high time = 50ns CAS falling to CAS falling = 150ns Refresh falling to CAS falling lowtime = 100ns or 150ns
RP	1	When set to 1 it extends RAS precharge time between consecutive VRAM cycles by 25ns. This parameter extends the nominal time from RAS falling to the next RAS falling by 50ns. Nominal RAS times are given below: When RP set to 0: RAS falling to RAS falling = 250ns (5 clock cycles) Refresh falling to RAS falling = 200ns When RP set to 1: RAS falling to RAS falling = 300ns (6 clock cycles) Refresh falling to RAS falling = 250ns **Note**: If both VA and RP are set to 1 then RAS falling to RAS falling = 350ns (7 clock cycles).
RA	2	When set to 1 it extends CAS and RAS active time for VRAM refresh cycles. This parameter determines the nominal time that CAS and RAS are active during a refresh cycle to the VRAM. Nominal CAS/RAS times are given below: When RA set to 0: CAS/RAS low time = 100ns When RA set to 1: CAS/RAS low time = 150ns

Table 21.17 Effects of setting the Memory configuration 1 register

Bit 1 (RP) determines the time between cycles. If set to 1 the **notVRAS0-1** low and high times are each extended by half a cycle. If set to 0 RAS would be high for a nominal time of 100ns.

Bit 2 (RA) only affects refresh cycles which are described on page 453.

Random cycles

The read data from the VRAM is latched into the IMS G200 using either **notVCAS0-1** or **notVOE** whichever becomes inactive first. This varies depending on the setting of the memory parameters. Figure 21.23 gives the cycle timings for various settings of the Memory configuration 1 register.

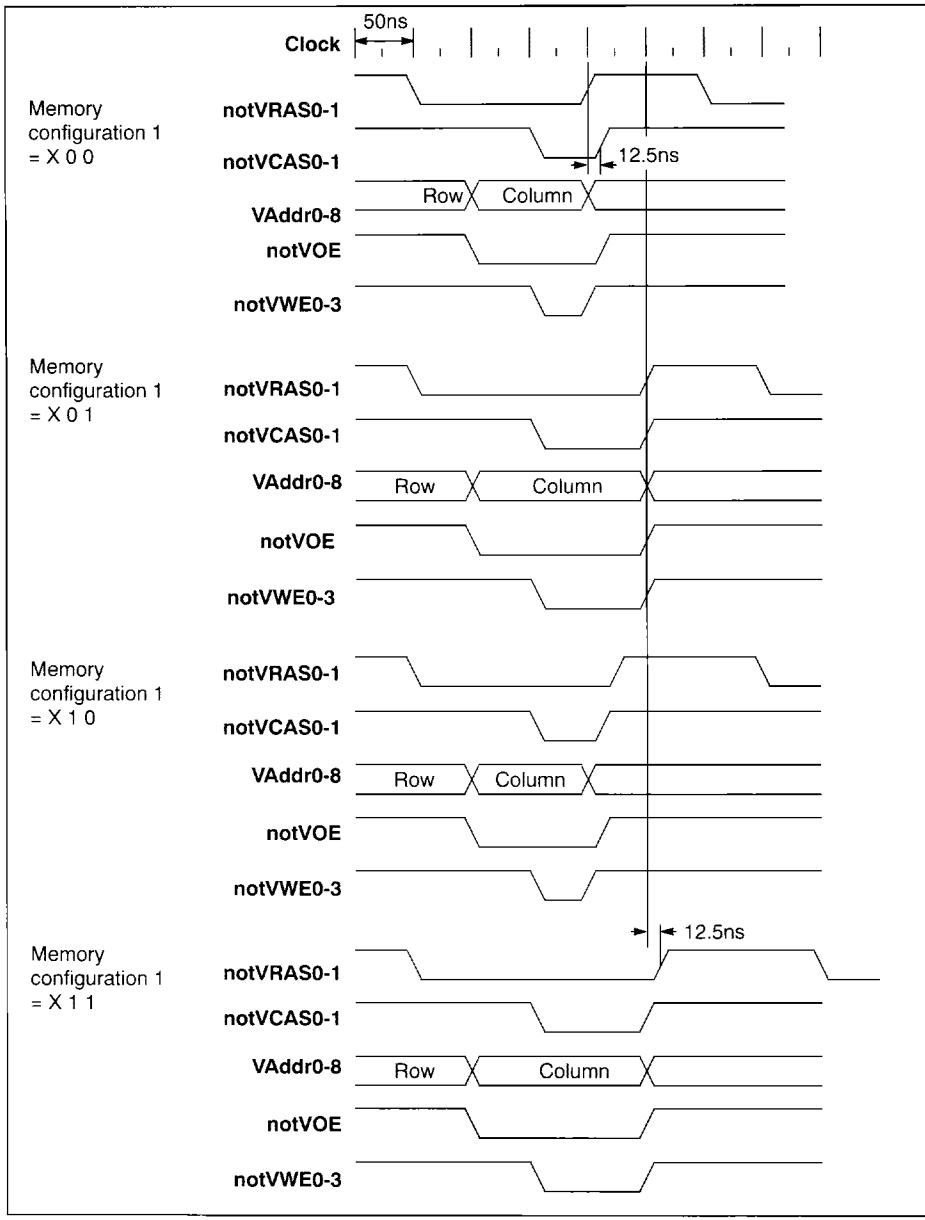


Figure 21.23 Random cycles -32 bit wide VRAMs for different Memory configuration 1 settings

Page mode cycles

Page mode cycles can occur for one of two reasons; either because the VRAM width does not enable the access to take place in one normal access (i.e. the VRAM width is less than 32 bits), or because the IMS G200 flags that there will be a paged mode access.

Figure 21.24 shows page mode cycle timings for different register settings.

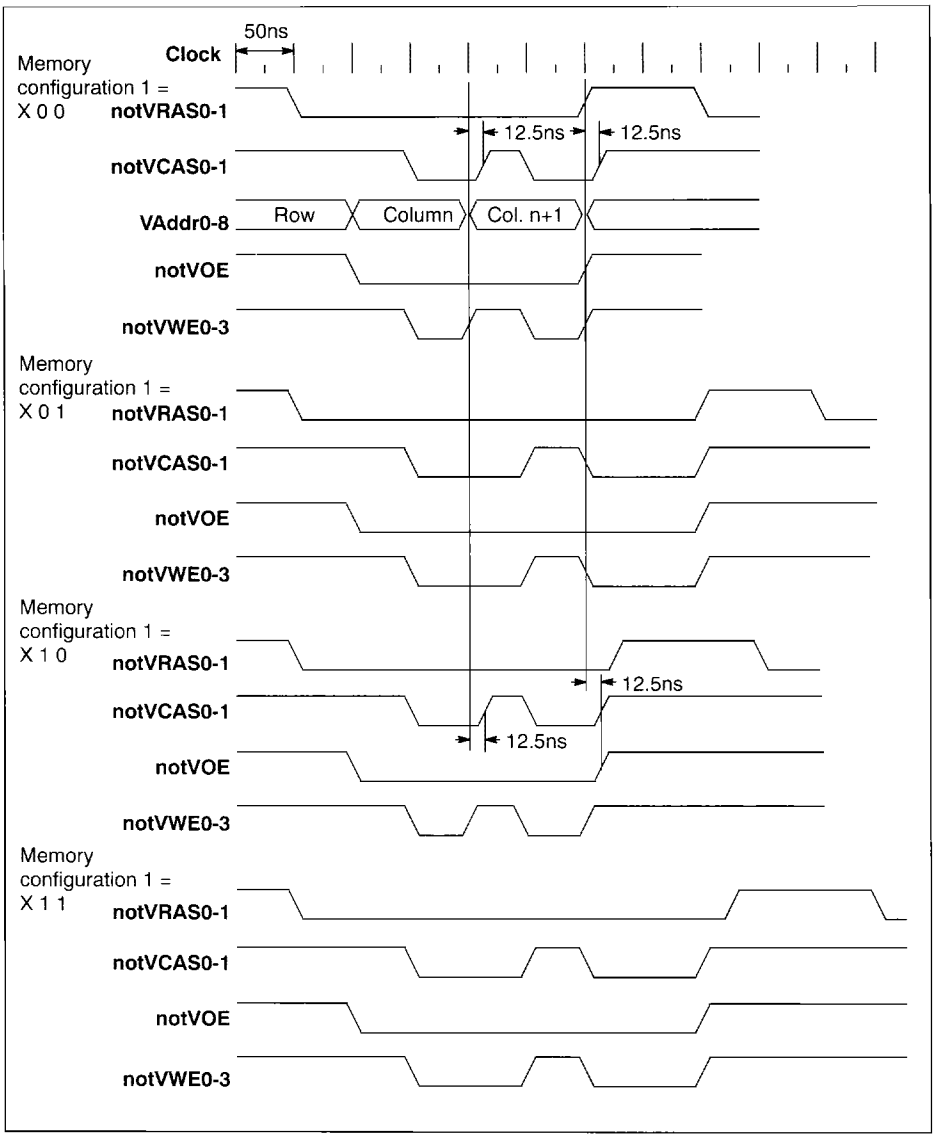


Figure 21.24 Page mode cycles - for different Memory configuration 1 settings

Refresh cycles

A CAS-before-RAS refresh cycle is used to refresh the VRAMs. The cycle can be extended by setting memory parameter index 1 (bit 3), thus extending the RAS/CAS active time by 50ns. The following diagram shows the timings for different settings of the **memory configuration 1** register (index 1).

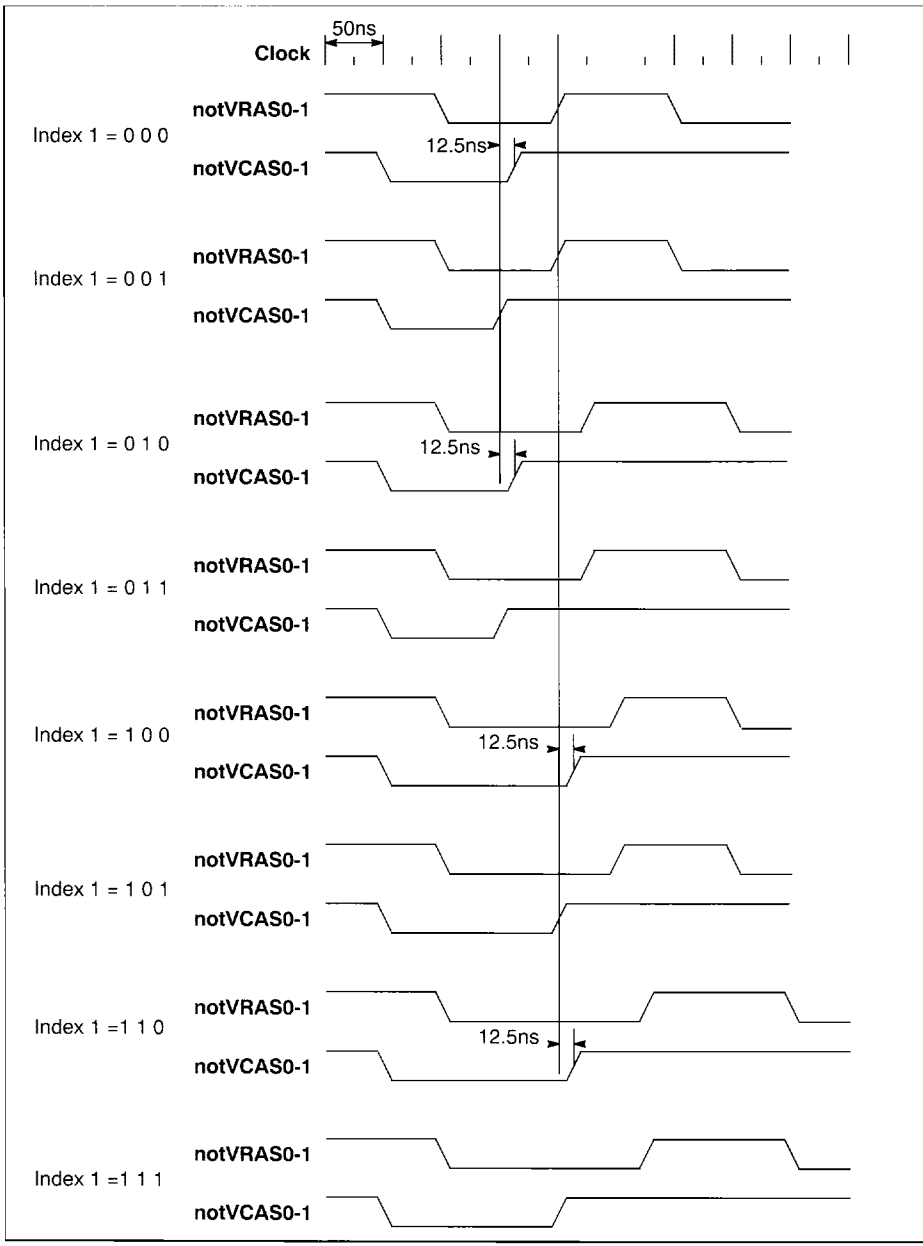


Figure 21.25 Refresh cycle timings for different settings of Memory configuration 1 register

Referencing of VRAM timings to the IMS G200 processor clock

As stated previously, all accesses on the random read/write port of the VRAMs are timed by and synchronous to the IMS G200 processor clock (**Clk**). Table 21.18 gives the absolute position of these strobes with respect to this clock.

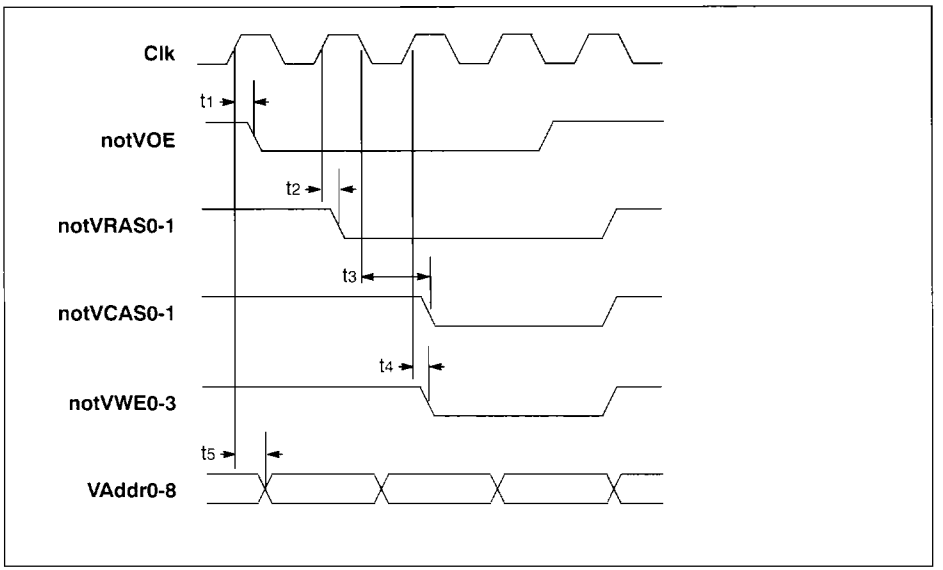


Figure 21.26 Referencing of VRAM timings to the IMS G200 processor clock

Symbol	Parameter	Min	Max	Unit	Notes
t1	**Clk** to **notVOE**	10	45	ns	
t2	**Clk** to **notVRAS0-1**	10	38	ns	
t3	**Clk** to **notVCAS0-1**	10	30	ns	
t4	**Clk** to **notVWE0-3**	10	20	ns	
t5	**Clk** to **VAddr0-8**	10	50	ns	

Table 21.18 VRAM timings

Transfer cycle timings

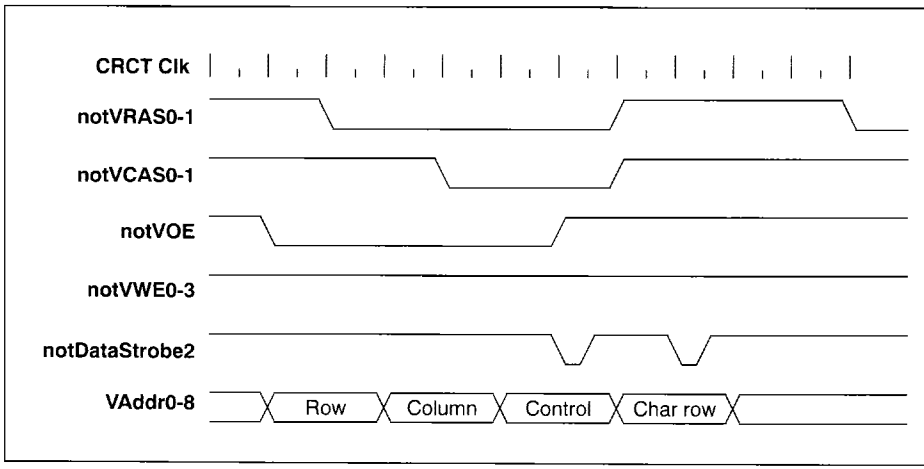


Figure 21.27 SAM load timing – basic transfer cycle

VRAM serial port interface timings

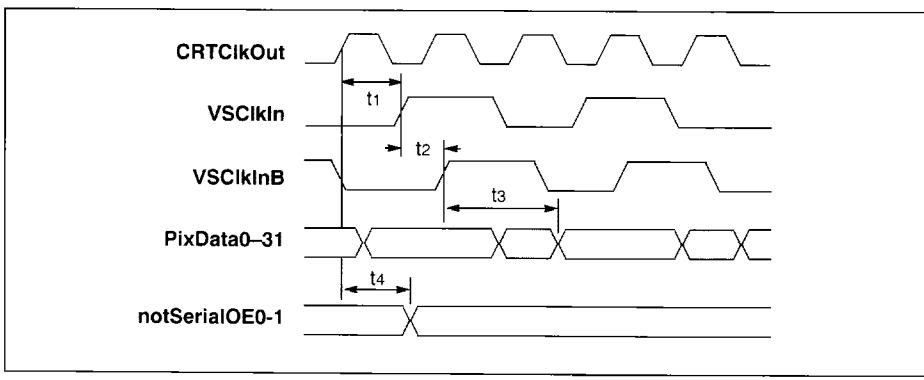


Figure 21.28 VRAM serial port interface timings diagram (see note 1, Table 21.19)

Symbol	Parameter	Min	Max	Units	Notes
t1	**CRTClkOut** high to **VSClkIn** high	-	25.6	ns	1
t2	On-card buffer delay	-	7.0	ns	1
t3	VRAM access time	-	35.0	ns	1
t4	IMS G191 **CRTClkOut** to IMS G200 **notSerialOE0-1**	-	28.0	ns	1

Note:
1 **CRTClkOut**, **VSClkIn**, **VSClkInB** and **PixData0-31** refer to IMS G191 pins

Table 21.19 VRAM serial port interface timings

21.11.3 IMS G191 interface timings

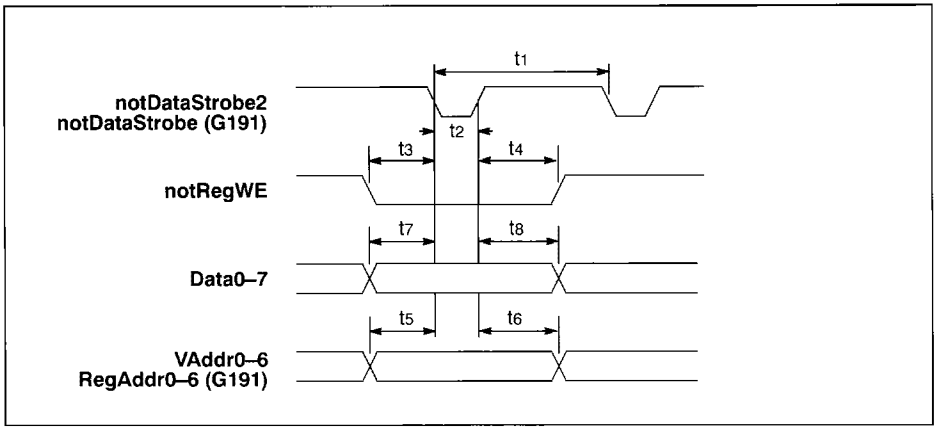


Figure 21.29 Write to IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe2** period - fast access	250.0		ns	
	notDataStrobe2 period - slow access	500.0		ns	
	notDataStrobe2 period - control codes	40.0		ns	
t2	**notDataStrobe2** width - fast access	100.0		ns	
	notDataStrobe2 width - slow access	150.0		ns	
	notDataStrobe2 width - control codes	20.0		ns	
t3	**notRegWE** set up to **notDataStrobe2**	50.0		ns	
t4	**notRegWE** hold after **notDataStrobe2**	40.0		ns	
t5	**VAddr0-6** set up to **notDataStrobe2**	40.0		ns	
t6	**VAddr0-6** hold after **notDataStrobe2**	40.0		ns	
t7	**Data0-7** set up to **notDataStrobe2**	40.0		ns	
t8	**Data0-7** hold after **notDataStrobe2**	40.0		ns	

Table 21.20 Write to IMS G191 register timings

Read from G191 register timings

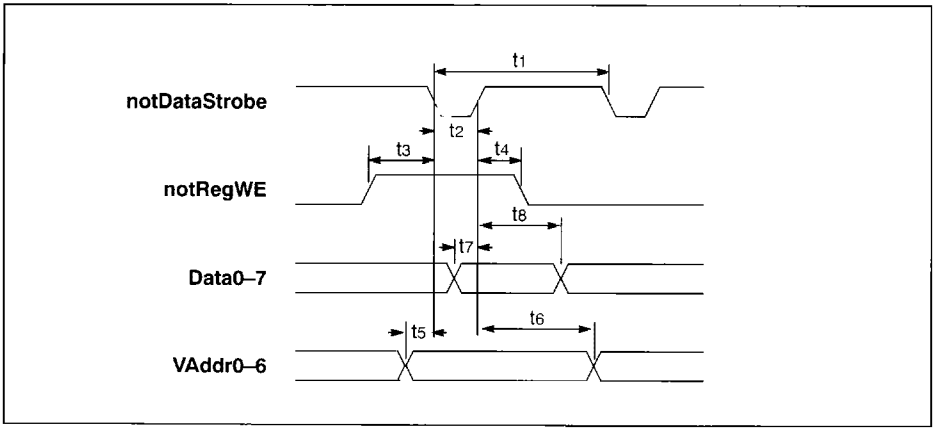


Figure 21.30 Read from IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe2** period - fast access	250.0		ns	
	notDataStrobe2 period - slow access	500.0		ns	
t2	**notDataStrobe2** width - fast access	100.0		ns	
	notDataStrobe2 width - slow access	150.0		ns	
t3	**notRegWE** set up to **notDataStrobe2**	40.0		ns	
t4	**notRegWE** hold after **notDataStrobe2**	40.0		ns	
t5	**VAddr0-6** setup to **notDataStrobe2**	40.0		ns	
t6	**VAddr0-6** hold after **notDataStrobe2**	40.0		ns	
t7	**Data0-7** read setup	40.0		ns	
t8	**Data0-7** hold after **notDataStrobe2**	0.0		ns	

Table 21.21 Read from IMS G191 register timings

21.11.4 CRT controller timings

CRTC clock timings

The CRTC clocks are generated by the IMS G191 and used by the IMS G200 to provide synchronization of signals between the IMS G200, VRAM and the IMS G191. Their frequency is set by bit 0 of the clock frequency select register.

The interface timing requirements of the clocks are given below. **CRTClkIn2** is half the frequency of **CRTClkIn**.

Video control timings

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G200 from the CRTC clocks and fed back into the IMS G191 via the **VideoCtrlIn0-1** pins.

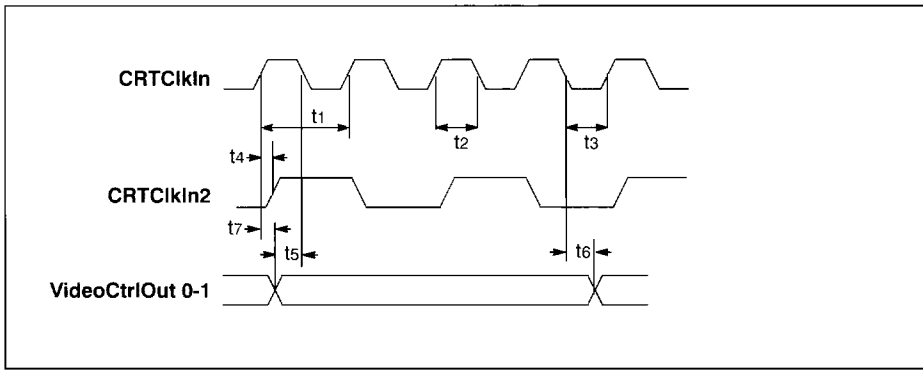


Figure 21.31 CRTC clock and video control timings

Symbol	Parameter	Min	Max	Units	Notes
t1	IMS G191 **CRTClkIn** period	22.0	50.0	ns	
t2	IMS G191 **CRTClkIn** pulse width high	8.0	32.0	ns	
t3	IMS G191 **CRTClkIn** pulse width low	8.0	32.0	ns	
t4	IMS G191 **CRTClkIn** to **CRTClkIn2** delay	–5.0	5.0	ns	
t5	**VideoCtrlOut0-1** setup time	5.0		ns	
t6	**VideoCtrlOut0-1** hold time	12.5		ns	
t7	IMS G191 **CRTClkIn** to **VideoCtrlOut0-1**		30	ns	

Table 21.22 CRTC clock timings

21.11.5 External memory timings

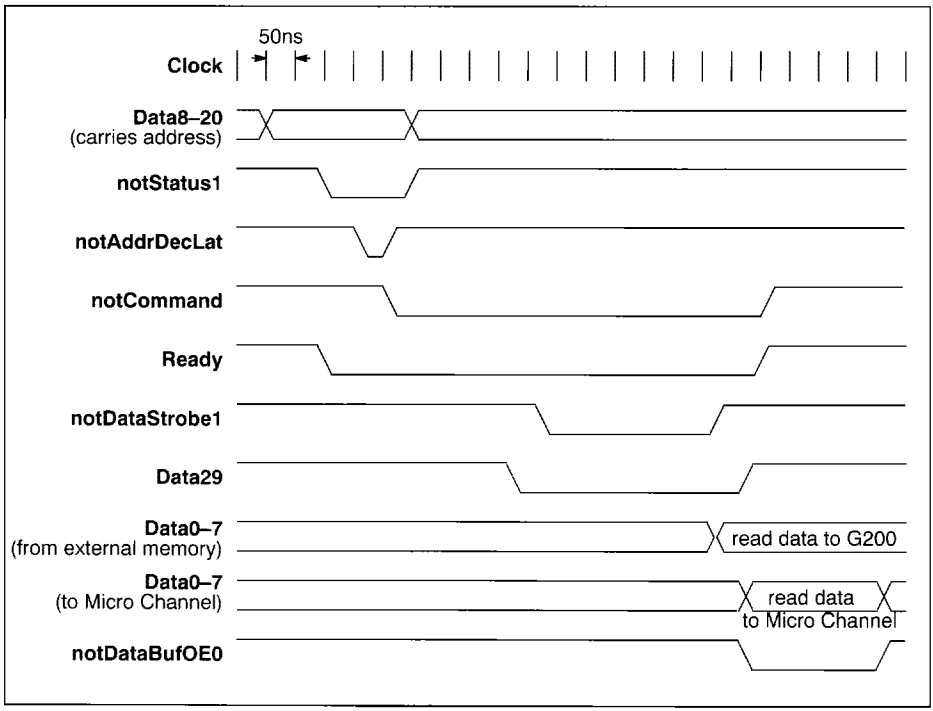


Figure 21.32 Read from external memory

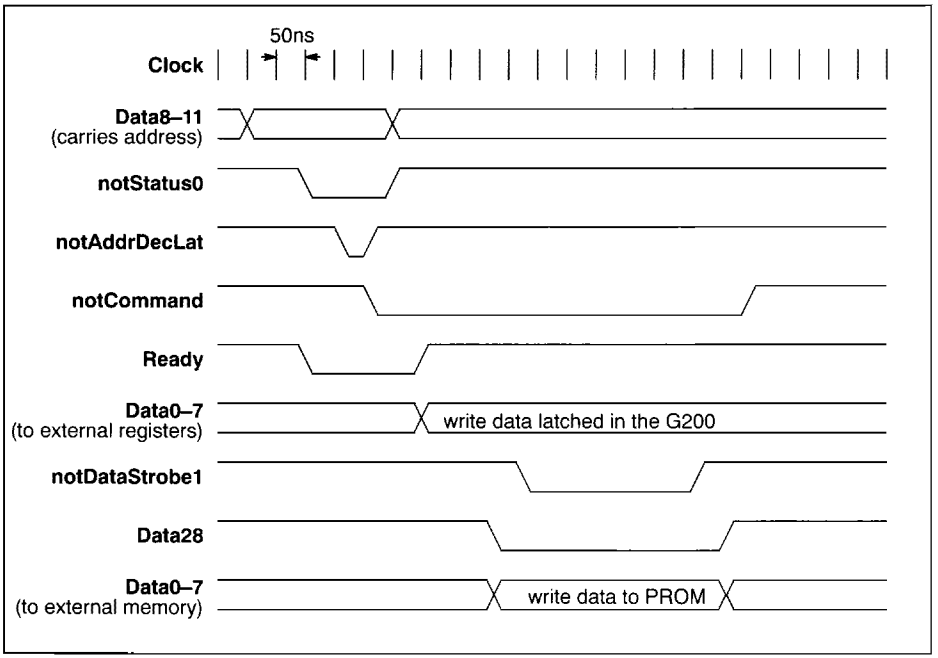


Figure 21.33 Write to external memory

21.11.6 External register timings

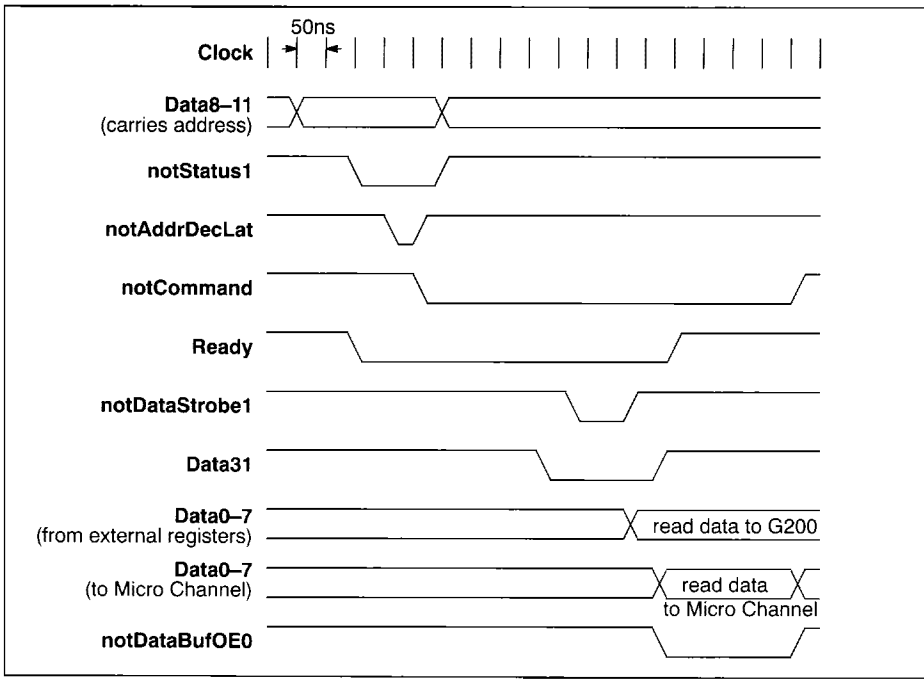


Figure 21.34 Read from external register

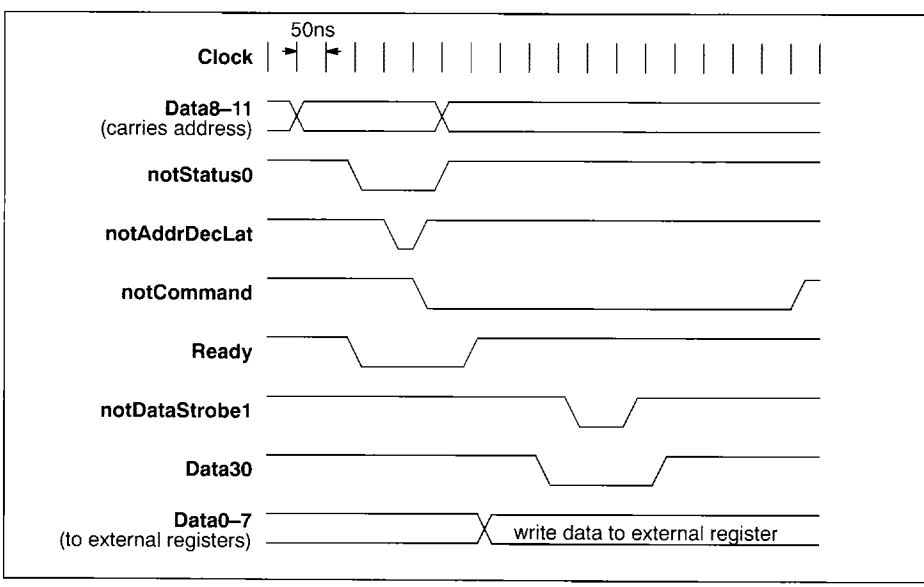


Figure 21.35 Write to external register

21.11.7 Reset timings

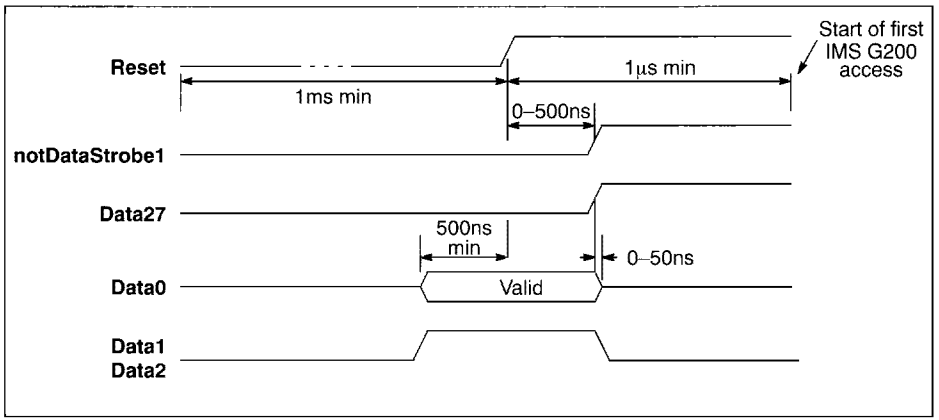


Figure 21.36 Reset timings

21.12 Electrical specifications

21.12.1 Absolute Maximum Ratings

Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply Voltage	0.0	7.5	Volts
V_I	Voltage on input pin	−1.0	V_{DD}+0.5	Volts
V_O	Voltage on output pin	−1.0	V_{DD}+0.5	Volts
T_S	Storage temperature	−65	150	°C
T_A	Temperature under bias	−55	125	°C

Table 21.23 Absolute maximum ratings

21.12.2 DC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply Voltage	4.5	5.5	Volts
T_A	Temperature under bias	0	70	°C
PD	Power dissipation		2	Watts
V_{IH}	Input logic '1' voltage	2.1	V_{DD}+0.5	Volts
V_{IL}	Input logic '0' voltage	−0.5	0.8	Volts
I_{IN}	Digital input current	−10	+10	μA

Table 21.24 DC operating conditions

Worst case timings are applicable only if the device is within the recommended parameters.

21.12.3 Pin output loading characteristics

Pin name	C_L (pF)	V_{OH} (Volts)		V_{OL} (Volts)		I_{OH} (mA)	I_{OL} (mA)	Rs (Ω)		Islew
	Max	Min	Max	Min	Max	Max	Max	Min	Max	Min
notBurst ArbOut0-3 notPreemptOut notIRQ notDataBufOE0-3 notCardSelFbk CoProcStat notCoProcStatOE	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notSerialOE0-1	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
VideoCtrlOut0-1 notDataStrobe2	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
MonHSync	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
Addr0-31 notByteEn0-3 notSysByteHiEn MemnotIO notStatus0-1	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	
notCommand notAddrDecLat	24	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	
notVRAS0-1	24	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
MemAddrEn24	25	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	
notVWE0-3	28	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notVCAS0-1	28	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Medium
notVOE	28	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
notStrDatStb	33	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
VAddr0-8	33	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
VSClkOut	36	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
Ready	40	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notDataStrobe1 AddrBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
DataBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
Data0-31	85	2.4	4.5	0.0	0.4	–0.7	8.0	20	30	Medium
MonVSync	168	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow

Table 21.25 IMS G200 pin output loading characteristics

Where,

C_L is the maximum load capacitance
V_{OH} is the high level output voltage
V_{OL} is the low level output voltage
I_{OH} is the high level output current
I_{OL} is the low level output current
Rs is the termination impedance
Islew is the current slew rate

21.13 Package specifications

184 pin plastic flat pack package

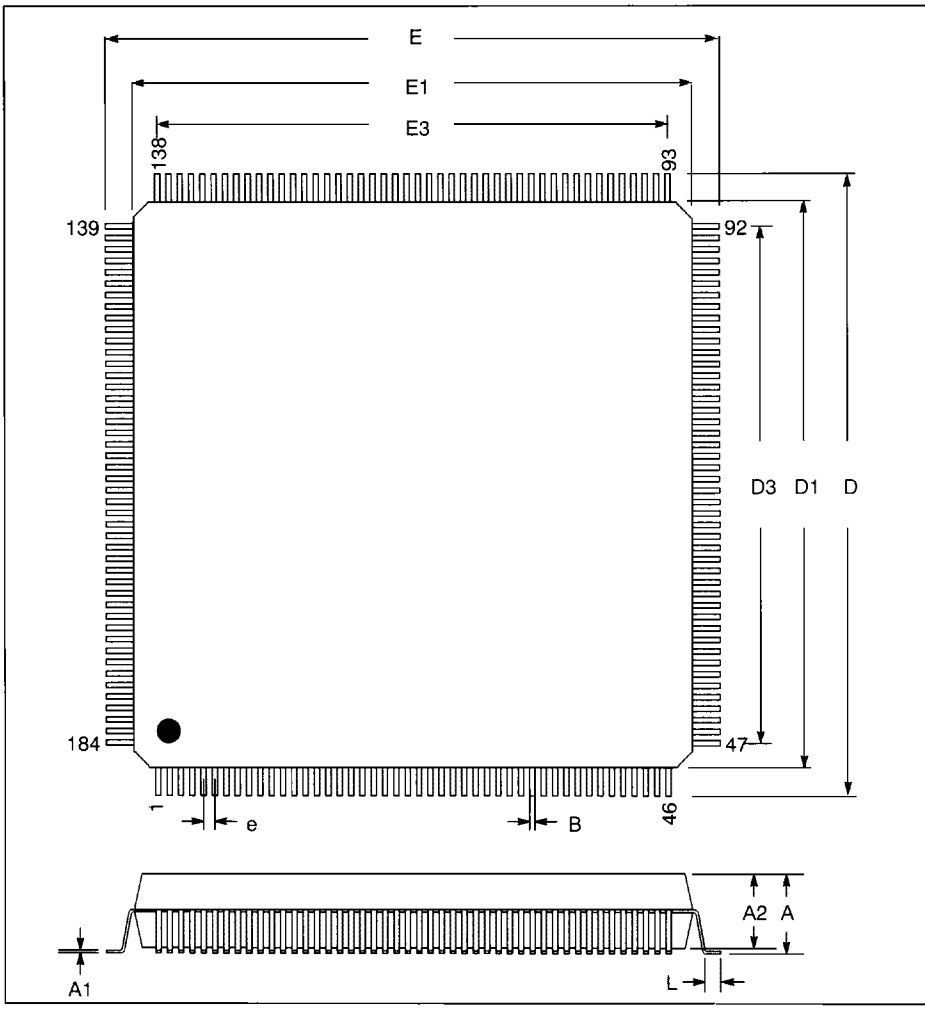


Figure 21.37 184 lead plastic quad flat pack

DIM	Millimeters			Inches			Notes
	MIN	NOM	MAX	MIN	NOM	MAX	
A			4.500			0.177	
A_1	0.100	0.150	0.200	0.004	0.006	0.008	
A_2		4.200			0.165		Ref.
D	34.950	35.20	35.450	1.376	1.386	1.396	
D_1	31.800	32.000	32.200	1.252	1.260	1.268	
D_3		29.250			1.151		Ref.
E	34.950	35.200	35.450	1.376	1.386	1.396	
E_1	31.800	32.000	32.200	1.252	1.260	1.268	
E_3		29.250			1.151		Ref.
L	0.650	0.800	0.950	0.026	0.032	0.038	
e		0.650			0.0256		BSC
B	0.200	0.300	0.400	0.008	0.012	0.016	

Table 21.26 184 lead plastic quad flat pack

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	VDD	47	VDD	93	VDD	139	notBurst
2	Addr2	48	Data8	94	VSClkOut	140	notIRQ
3	Addr3	49	Data9	95	notVRAS0	141	Ready
4	Addr4	50	Data10	96	GND	142	GND
5	Addr5	51	Data11	97	notVRAS1	143	notStrDatStb
6	Addr6	52	GND	98	notSerialOE0	144	notCommand
7	GND	53	Data12	99	notSerialOE1	145	VDD
8	Addr7	54	Data13	100	GND	146	notAddrDecLat
9	Addr8	55	Data14	101	notVWE0	147	GND
10	Addr9	56	Data15	102	VDD	148	notStatus0
11	Addr10	57	Data16	103	notVWE1	149	notStatus1
12	Addr11	58	Data17	104	notVWE2	150	HoldToGND
13	Addr12	59	Data18	105	GND	151	notStrDatReq0
14	Addr13	60	Data19	106	notVWE3	152	notStrDatReq1
15	Addr14	61	GND	107	N/C	153	notDSize16Rtn
16	Addr15	62	Data20	108	VideoCtrlOut0	154	notDSize32Rtn
17	Addr16	63	Data21	109	GND	155	ReadyRtn
18	GND	64	Data22	110	VideoCtrlOut1	156	notPreemptIn
19	Addr17	65	Data23	111	VDD	157	ArbIn0
20	Addr18	66	VDD	112	notDataStrobe2	158	ArbIn1
21	Addr19	67	Data24	113	notDataStrobe1	159	ArbIn2
22	Addr20	68	Data25	114	GND	160	ArbIn3
23	VDD	69	VDD	115	VDD	161	VDD
24	GND	70	GND	116	GND	162	GND
25	Addr21	71	Data26	117	MonHSync	163	VDD
26	VDD	72	Data27	118	MonVSync	164	GND
27	Addr22	73	GND	119	DataBufDir	165	ArbGrant
28	Addr23	74	Data28	120	GND	166	notRefresh
29	Addr24	75	Data29	121	notDataBufOE0	167	notSetup
30	Addr25	76	Data30	122	notDataBufOE1	168	CRTClkIn2
31	Addr26	77	Data31	123	VDD	169	CRTClkIn
32	GND	78	VAddr0	124	notDataBufOE2	170	MonSyncOE
33	Addr27	79	VAddr1	125	notDataBufOE3	171	Reset
34	Addr28	80	VAddr2	126	GND	172	Clk
35	Addr29	81	VAddr3	127	ArbOut0	173	HoldToGND
36	Addr30	82	VAddr4	128	ArbOut1	174	HoldToVDD
37	Addr31	83	VDD	129	ArbOut2	175	notSysByteHiEn
38	Data0	84	GND	130	ArbOut3	176	notByteEn0
39	Data1	85	VAddr5	131	GND	177	notByteEn1
40	Data2	86	VAddr6	132	notCoProcStatOE	178	notByteEn2
41	Data3	87	VAddr7	133	CoProcStat	179	notByteEn3
42	GND	88	VAddr8	134	VDD	180	GND
43	Data4	89	notVCAS0	135	AddrBufDir	181	MemnotIO
44	Data5	90	notVCAS1	136	notPreemptOut	182	MemAddrEn24
45	Data6	91	GND	137	GND	183	Addr0
46	Data7	92	notVOE	138	notCardSelFbk	184	Addr1

Table 21.27 IMS G200 184 pin PQFP package pinout by pin number

Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin
Addr0	183	Data1	39	GND	109	notSetUp	167
Addr1	184	Data2	40	GND	114	notStatus0	148
Addr2	2	Data3	41	GND	116	notStatus1	149
Addr3	3	Data4	43	GND	120	notStrDatReq0	151
Addr4	4	Data5	44	GND	126	notStrDatReq1	152
Addr5	5	Data6	45	GND	131	notStrDatStb	143
Addr6	6	Data7	46	GND	137	notSysByteHiEn	175
Addr7	8	Data8	48	GND	142	notVCAS0	89
Addr8	9	Data9	49	GND	147	notVOE	92
Addr9	10	Data10	50	GND	162	notVRAS0	95
Addr10	11	Data11	51	GND	164	notVWE0	101
Addr11	12	Data12	53	GND	180	notVWE1	103
Addr12	13	Data13	54	HoldToGND	150	notVWE2	104
Addr13	14	Data14	55	HoldToGND	173	notVWE3	106
Addr14	15	Data15	56	HoldToVDD	174	Ready	141
Addr15	16	Data16	57	MemAddrEn24	182	ReadyRtn	155
Addr16	17	Data17	58	MemnotIO	181	Reset	171
Addr17	19	Data18	59	MonHSync	117	CoProcStat	133
Addr18	20	Data19	60	MonSyncOE	170	VAddr0	78
Addr19	21	Data20	62	MonVSync	118	VAddr1	79
Addr20	22	Data21	63	N/C	90	VAddr2	80
Addr21	25	Data22	64	N/C	97	VAddr3	81
Addr22	27	Data23	65	N/C	107	VAddr4	82
Addr23	28	Data24	67	notAddrDecLat	146	VAddr5	85
Addr24	29	Data25	68	notBurst	139	VAddr6	86
Addr25	30	Data26	71	notByteEn0	176	VAddr7	87
Addr26	31	Data27	72	notByteEn1	177	VAddr8	88
Addr27	33	Data28	74	notByteEn2	178	VDD	1
Addr28	34	Data29	75	notByteEn3	179	VDD	23
Addr29	35	Data30	76	notCardSelFbk	138	VDD	26
Addr30	36	Data31	77	notCommand	144	VDD	47
Addr31	37	DataBufDir	119	notCoProcStatOE	132	VDD	66
AddrBufDir	135	GND	7	notDataBufOE0	121	VDD	69
ArbGrant	165	GND	18	notDataBufOE1	122	VDD	83
ArbIn0	157	GND	24	notDataBufOE2	124	VDD	93
ArbIn1	158	GND	32	notDataBufOE3	125	VDD	102
ArbIn2	159	GND	42	notDataStrobe1	113	VDD	111
ArbIn3	160	GND	52	notDataStrobe2	112	VDD	115
ArbOut0	127	GND	61	notDSize16Rtn	153	VDD	123
ArbOut1	128	GND	70	notDSize32Rtn	154	VDD	134
ArbOut2	129	GND	73	notIRQ	140	VDD	145
ArbOut3	130	GND	84	notPreemptIn	156	VDD	161
Clk	172	GND	91	notPreemptOut	136	VDD	163
CRTClkIn	169	GND	96	notRefresh	166	VideoCtrlOut0	108
CRTClkIn2	168	GND	100	notSerialOE0	98	VideoCtrlOut1	110
Data0	38	GND	105	notSerialOE1	99	VSClkOut	94

Table 21.28 IMS G200 184 pin PQFP package pinout by signal name

21.14 Ordering information

Device	Clock rate	Package	Part number
IMS G200	40MHz	184 pin plastic quad flat pack	IMS G200X-40S