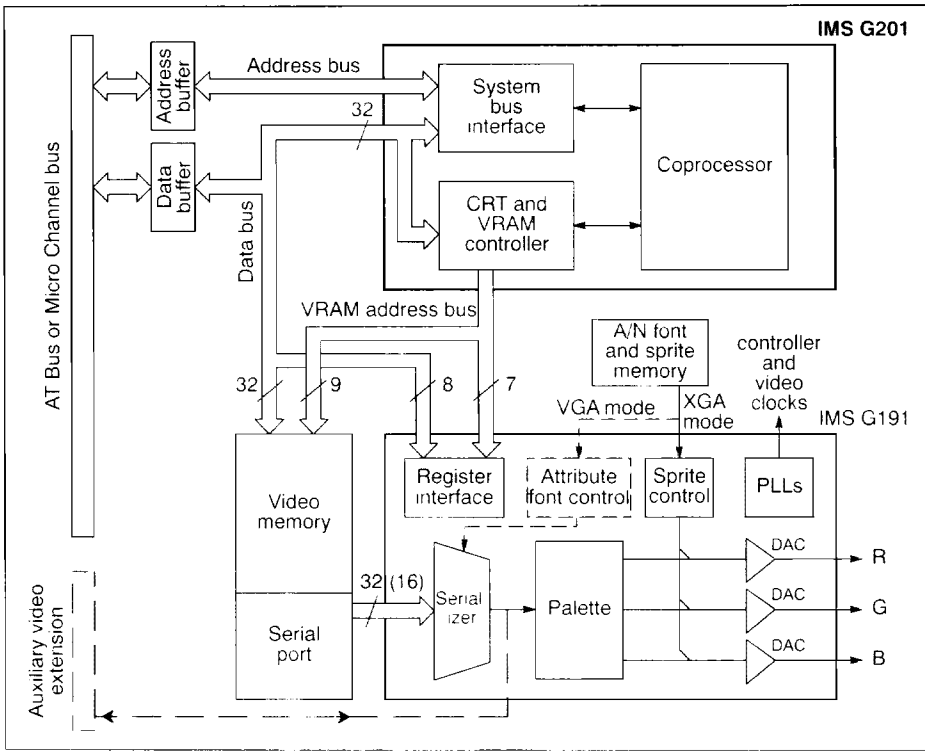
XGA DISPLAY CONTROLLER

PRELIMINARY INFORMATION



FEATURES

Supports both AT Bus and Micro Channel interfaces
Allows 2-chip AT Bus or Micro Channel bus XGA solution (IMS G201 + IMS G191)
Bus mastership on AT Bus and Micro Channel
VGA and XGA standard registers
Programmable CRT controller supports many display modes including:
- 1280×1024 with 16/256 colors (interlaced)
- 1024×768 with 256 colors (non-interlaced)
- 800×600 with 65.536 colors (non-interlaced)

132 column text mode (1056×480 resolution)
16 bit true color support (5 Red, 6 Green, 5 Blue)
Video RAM interface for high performance
ISO-compliant screen refresh rates
Fully backwards compatible with IMS G200 XGA display controller
208 pin PQFP package
IMS G201 coprocessor supports:
- 1, 2, 4, 8 and 16 bit Pixel and bit block transfers
- Line drawing
- Area filling
- Logical and arithmetic pixel mixing
- Pixel map masking
- Scissoring
- X, Y axis addressing

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22.1 IMS G201 description

The IMS G201 display controller chip comprises the system bus interface, drawing coprocessor, and the memory and display controller components of the G201/G191 chipset based XGA subsystem.

System bus interface modes

The IMS G201 can be set to operate in one of two modes: AT bus mode or Micro Channel mode.

In AT bus mode it is designed to interface with an AT bus standard and supports a 16 bit or an 8 bit interface. It supports both slave and master operations for a 16 bit interface or slave operations only for an 8 bit interface. A block diagram showing the IMS G201 in AT bus mode is given in Section 22.1.1.

In Micro Channel bus mode the IMS G201 is designed to interface to a Micro Channel bus standard and supports a 32 or a16 bit interface. It operates both as slave and master. Streaming data (100ns cycle) operation is supported when the IMS G201 is a master only. A block diagram showing the IMS G201 in Micro Channel bus mode is given in Section 22.1.2.

22.1.1 Detailed IMS G201 block diagram for AT bus mode

Figure 22.1 shows the main functional units and all pin connections of the IMS G201 in AT bus mode.

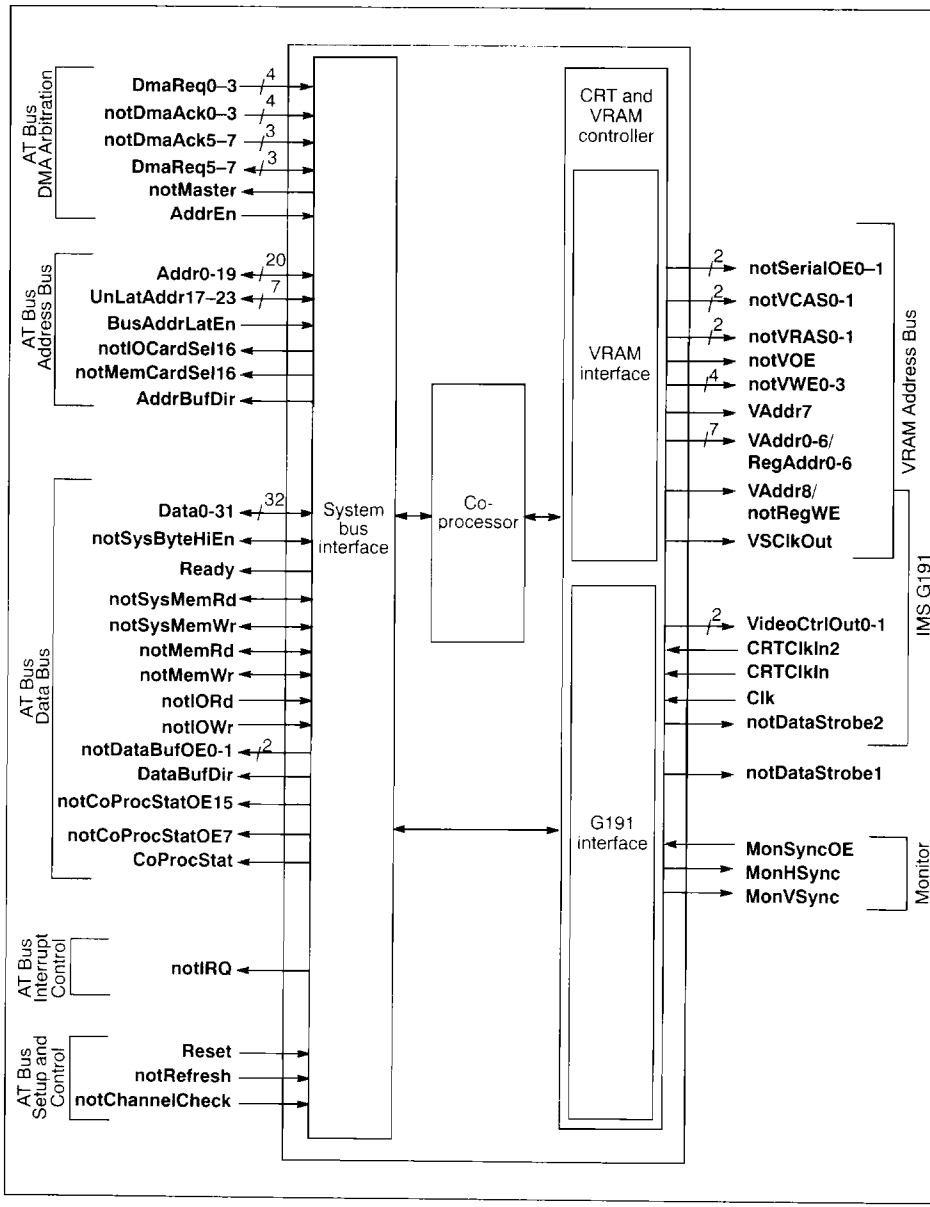

Figure 22.1 IMS G201 block diagram for AT bus mode

22.1.2 Detailed IMS G201 block diagram for Micro Channel bus mode

Figure 22.2 shows the main functional units and all pin connections of the IMS G201 in Micro Channel bus mode.

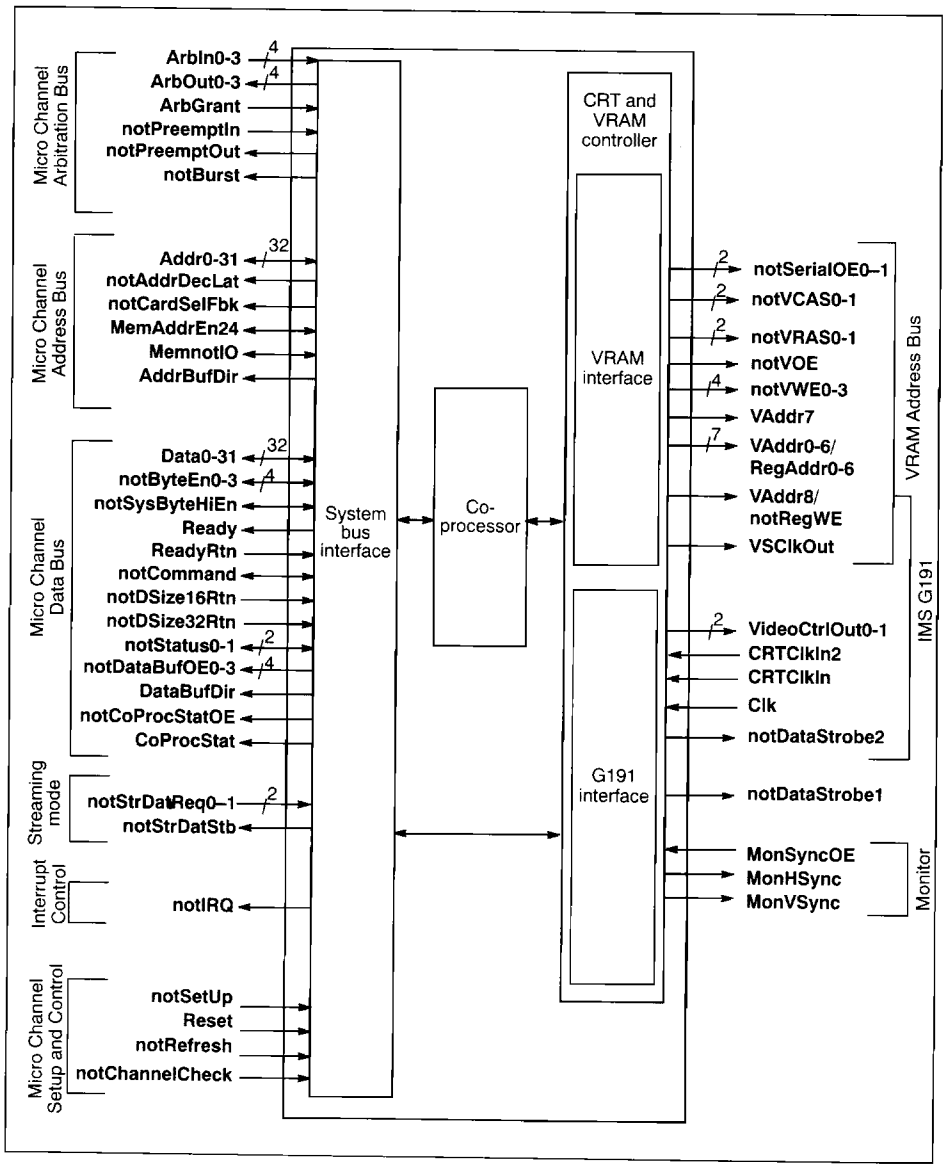

Figure 22.2 IMS G201 block diagram for Micro Channel bus mode

22.2 Pin function reference guide

Signal names are prefixed by **not** if they are active low, otherwise they are active high.

22.2.1 System bus interface

The pins on the system bus interface are dual function. The function of the pins is dependent on whether it is interfacing to an AT bus or a Micro Channel bus. The sub-section below lists the pin descriptions when the IMS G201 is operating in AT bus mode, this is followed by a separate sub-section detailing the pins when in Micro Channel mode.

AT bus mode

AT bus Address bus

Pin name	I/O	Signal description
Addr0-19	I/O	These address signals are generated by the microprocessor or DMA controller and are gated on the system bus when **BusAddrLatEn** is high. They are used by the AT bus interface logic for register decoding.
UnLatAddr17–23	I/O	These signals generate memory decodes for 16 bit, 1 wait state, memory cycles and may be derived from the system microprocessor or other arbitrated devices or DMA controllers.
BusAddrLatEn	I	This signal indicates a valid microprocessor or DMA address and is used for address latching.
notIOCardSel16	O	This signal indicates to the system that the current data transfer is a 16 bit 1 wait state, I/O cycle. It is derived from the decode of **UnLatAddr0–15** and is driven with a tri-state driver capable of sinking 20mA.
notMemCardSel16	O	This signal indicates to the system that the current data transfer is a 16 bit 1 wait state, memory cycle. It is derived from the decode of **UnLatAddr17–23** and is driven with a tri-state driver capable of sinking 20mA.
AddrBufDir	O	This pin controls the direction of an external 3 state bidirectional buffer isolating the IMS G201 from the AT bus. Active high signifies the AT bus is driving the IMS G201 pins (G201 is the slave), and active low signifies that IMS G201 is driving the AT bus (G201 is the master).

AT bus Arbitration bus

Pin name	I/O	Signal description
DmaReq5–7	I/O	These signals asynchronously request a bus master service. They are prioritized with **DmaReq5** having highest priority and **DmaReq7** having lowest.
notDmaAck5–7	I	A DMA request is is serviced after an arbitration acknowledge generated on **notDmaAck5–7.**
DmaReq0–3	I	The 8-bit DMA resources are used to monitor DMA activity on the bus for Pacing control.
notDmaAck0–3	I	A DMA request is is serviced after an arbitration acknowledge generated on **notDmaAck0–3.** The 8-bit DMA resources are used to monitor DMA activity on the bus for internal Pacing control of the IMS G201.
notMaster	O	This signal is used with a **DmaReq** line to gain control of the system. Typically an arbitrating controller (the IMS G201) on the I/O channel may assert this signal to allow control of the system address, data and control lines.
AddrEn	I	When active, the address enable signal **AddrEn** tri-states the microprocessor and other devices from the I/O channel to allow DMA transfers to take place.

AT bus Data bus

Pin name	I/O	Signal description
Data0-15	I/O	The **Data15** signal line represents the most significant bit and **Data0** the least significant bit of the AT data bus. The data pins are shared by the VRAM random data port and the AT bus. The data pins may connect directly to the VRAM but must be isolated from the AT bus by suitable bi-directional three-state drivers.
Data16-31		This portion of the data bus completes the unbuffered 32-bit connection (**Data0-31**) to the VRAM random port.
Data8-11		**Data8-11** are also used to carry an address for external registers.
Data8-26		**Data8-26** are also used to carry an address for external memory (typically EPROM). **Data23-26** correspond to bits 2-5 in the ROM paging register in AT bus mode.
Data27		**Data27** (with **notDataStrobe1**) is also a strobe qualifier for chip configuration data.
Data28		**Data28** is also a strobe qualifier for writes to external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory write.
Data29		**Data29** is also a strobe qualifier for reads from external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory read.
Data30		**Data30** is also a strobe qualifier for external register writes. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register write.
Data31		**Data31** is also a strobe qualifier for external register reads. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register read.

Pin name	I/O	Signal description
notSysByteHIEn	I/O	System byte high enable signal indicates the transfer of data on the high byte of the data bus (**Data8-15**). 16 bit devices use **notSysByteHIEn** to condition the respective data buffers.
Ready	I/O	The **Ready** signal allows resources to indicate to the bus owner that additional cycle time is required. If the **Ready** signal is not driven inactive, the cycle either is a no wait state or a standard cycle. If the **Ready** signal is driven inactive, the cycle length is extended until the line is driven active again.
notSysMemRd	I	This signal instructs memory devices to drive data onto the data bus. **notSysMemRd** is active only when the memory decode is within the low 1Mbyte of memory space.
notSysMemWr	I	This signal instructs memory devices to store the data present on the data bus. **notSysMemWr** is active only when the memory decode is within the low 1Mbyte of memory space.
notMemRd	I/O	This signal instructs the memory devices to drive data onto the data bus. **notMemRd** is active on all memory read cycles.
notMemWr	I/O	This signal instructs the memory devices to store data present on the data bus. **notMemWr** is active on all memory read cycles.
notIORd	I	This signal instructs an I/O device to drive its data onto the data bus.
notIOWr	I	This signal instructs an I/O device to store data on the data bus.
notDataBufOE0-1	O	A low on this signal puts the AT data bus isolation buffer in the active state; a high puts it in high impedance state. Bit 0 controls data bus bits 0:7, bit 1 controls data bus bits 8:15.
DataBufDir	O	This signal controls the direction of an external bidirectional three state transceiver isolating the AT data bus from the shared VRAM data bus. A low indicates drive towards the AT data bus. A high indicates drive towards the IMS G201 and VRAM.
notCoProcStatOE15	O	When active low this signal enables the output of a 3-state driver that connects the **CoProcStat** pin to bit 15 of the AT data bus.
notCoProcStatOE7	O	When active low this signal enables the output of a 3-state driver that connects the **CoProcStat** pin to bit 7 of the AT data bus.
CoProcStat	O	The **CoProcStat** signal indicates whether the coprocessor is busy (active high), or not (active low). The signal in conjunction with **notCoProcStatOE7** and **notCoProcStatOE15** provides a means of testing the coprocessor status without interrupting the coprocessor to allow the host CPU to use shared VRAM data bus.

AT bus Interrupt control

Pin name	I/O	Signal description
notIRQ	O	Interrupt request

AT bus Setup and control

Pin name	I/O	Signal description
notRefresh	I	This signal is used to indicate a memory refresh operation is in progress.
notChannelCheck	I	This signal is a general error condition. It can be driven active by any resource.
Reset	I	Bus reset
Clk	I	Clock

Micro Channel mode

For a full description of the functions of the Micro Channel pins refer to the *IBM PS/2 hardware technical reference manual*.

Micro Channel Address bus

Pin name	I/O	Signal description
Addr0-31	I/O	Address bus to communicate with the Micro Channel address bus. **Addr0** is the least significant bit (LSB) and **Addr31** is the most significant bit (MSB). These lines must be buffered externally to meet minimum drive requirements of the Micro Channel.
MemAddrEn24	I/O	Memory address enable 24 bits. This line indicates when an extended address is used on the bus. When **MemAddrEn24** is active this indicates that an unextended 24 bit address for less than or equal to 16 Mbytes is being presented.
notCardSelFbk	O	Card selected feedback. When the controlling master (e.g. i386 processor) addresses the G201, the G201 drives **notCardSelFbk** active to indicate its presence at the address specified.
notAddrDecLat	I/O	Address latch bus signal.
MemnotIO	I/O	Pin to distinguish between a memory cycle and an input/output (I/O) cycle. When **MemnotIO** is high a memory cycle is in progress, when low an I/O is in progress.
AddrBufDir	O	This pin controls the direction of external buffers between the IMS G201 host address bus pins and the micro channel bus. Active low indicates drive towards the host system bus, and active high towards the IMS G201.

Micro Channel Arbitration bus

Pin name	I/O	Signal description
ArbOut0-3	O	These outputs drive the Micro Channel arbitration bus priority levels. These signals must be buffered by an open collector device to meet Micro Channel requirements.
ArbIn0-3	I	These inputs are the Arbitration bits from the Micro Channel bus to enable the IMS G201 to control the bus in bus master mode.
ArbGrant	I	Arbitration grant signal.
notPreemptOut	O	This is the output portion of the Micro Channel **–PREEMPT** signal. This signal must be buffered by an open collector or three-state device to comply with Micro Channel convention.
notPreemptIn	I	**notPreemptIn** is logically tied directly to the Micro Channel **–PREEMPT** signal. This signal in conjunction with **notPreemptOut** mimics the open collector driver specified for **–PREEMPT** in the Micro Channel definition. It is used when the IMS G201 is operating in bus master mode.
notBurst	O	This signal indicates to the central arbitration control point the extended use of the channel for transferring a block of data. This type of data transfer is called a burst cycle. This signal must be buffered by an open collector or three-state device to comply with the Micro Channel specification.

Micro Channel Data bus

Pin name	I/O	Signal description
Data0-31	I/O	Data bits 0 to 31. **Data0** is the LSB and **Data31** is the MSB. The data pins are shared by the VRAM random data port and the Micro Channel data bus. They may connect directly to the VRAM but must be isolated from the Micro Channel by suitable bidirectional three-state drivers.
Data8-11		**Data8-11** are also used to carry an address for external registers.
Data8-26		**Data8-26** are also used to carry an address for external memory (typically EPROM). **Data21-26** correspond to bits 0-5 in the ROM paging register in Micro Channel bus mode.
Data27		**Data27** (with **notDataStrobe1**) is also a strobe qualifier for chip configuration data.
Data28		**Data28** is also a strobe qualifier for writes to external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory write.
Data29		**Data29** is also a strobe qualifier for reads from external memory. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external memory read.
Data30		**Data30** is also a strobe qualifier for external register writes. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register write.
Data31		**Data31** is also a strobe qualifier for external register reads. A low on this signal when the **notDataStrobe1** pin pulses low indicates an external register read.
DataBufDir	O	This signal controls the direction of an external bidirectional three state transceiver isolating the Micro Channel data bus from the shared VRAM data bus. A low indicates drive towards the Micro Channel data bus. A high indicates drive towards the IMS G201 and VRAM.
notDataBufOE0-3	O	A low on this signal puts the external Micro Channel data bus isolation buffer in the active state; a high puts it in high impedance state. Bit 0 controls data bus bits 0:7, bit 1 controls data bus bits 8:15, bit 2 controls data bus bits 16:23, and bit 3 controls data bus bits 24:31.
notCommand	I/O	This signal is used to define when data is valid on the data bus.
Ready	O	This normally active signal is pulled inactive (not ready) by the IMS G201 to allow additional time to complete a Micro Channel operation.
ReadyRtn	I	A positive AND of all the Micro Channel CD CHRDY (Ready) signals.
CoProcStat	O	The **CoProcStat** pin is an external output of 7 (BSY) of the External Polling Register (offset 11 in coprocessor address space). This provides an additional method of reading the coprocessor busy status without halting its operation (as would happen if the status was read via the coprocessor data bus). **CoProcStat** should be connected through a tri-state buffer to **Data15** (or **Data7** on an 8 bit bus).
notCoProcStatOE	O	This pin provides the enable input for the tri-state buffer that connects the **CoProcStat** pin to bit 15 of the host data bus (host side of the data buffer's transceivers).

Pin name	I/O	Signal description
notStatus0-1	I/O	Status bits 0 and 1. These lines indicate the start of a cycle and also define the type of cycle. Used in conjunction with the **MemnotIO** pin memory read/write operations are distinguished from I/O read/write operations as defined below:

MemnotIO	notStatus0	notStatus1	Function
0	0	1	I/O write
0	1	0	I/O read
1	0	1	memory write
1	1	0	memory read

notDSize16Rtn	I	Data size 16 bits return. This signal is provided to allow the controlling master to monitor the data size information.
notDSize32Rtn	I	Data size 32 bits return. This signal is provided to allow the controlling master to monitor the data size information.
notSysByteHiEn	I/O	System byte high enable. This line indicates and enables transfer of data on the high byte of the data bus (**Data8-15**) and is used with **Addr0** to distinguish between high byte transfers (**Data8-15**) and low byte transfers (**Data0-7**).
notByteEn0-3	I/O	Byte enables (used in conjunction with 32-bit bus cycles).

Micro Channel Interrupt control

Pin name	I/O	Signal description
notIRQ	O	Interrupt request

Micro Channel Setup and control

Pin name	I/O	Signal description
notRefresh	I	This signal is used to indicate a memory refresh operation is in progress.
notChannelCheck	I	This signal is a general error condition. It can be driven active by any resource.
notSetup	I	Micro Channel bus setup
Reset	I	Bus reset
Clk	I	Clock

Micro Channel Streaming mode

Pin name	I/O	Signal description
notStrDatStb	O	Connects to the Micro Channel –SD STB signal. **notStrDatStb** is driven by the IMS G201 (acting as the bus master) and serves as a clock, delimiting words in a streaming data transfer.
notStrDatReq0-1	I	Connects to the Micro Channel –SDR(0,1) signals. –SDR(0,1) are driven by the bus slave, following the activation of the Address Data Latch signal, to indicate that it supports streaming data.

22.2.2 VRAM interface

Pin name	I/O	Signal description
VAddr0-8	O	These pins have different functions depending on the operation. **VAddr0-8** carry the row and column addresses to the VRAMs to be strobed by the appropriate **RAS** or **CAS** signal.
VAddr0-6		**VAddr0-6** lines are also used to send the address of the IMS G191 parameter registers to the IMS G191.
VAddr8 / notRegWE		**VAddr8** is also used as a **notRegWE** pin to indicate to the IMS G191 whether the IMS G191 addressed register is being written to or read from. A high on this signal indicates a read from the register, a low indicates a write to the register.
notSerialOE0-1	O	Serial output enable strobes for multiplexing data from any one of four VRAM serial ports.
notVCAS0-1	O	VRAM column address strobes.
notVRAS0-1	O	VRAM row address strobes.
notVWE0-3	O	Write Enable control for VRAM data. A low indicates a write operation. Bit 0 controls **Data 0-7** Bit 1 controls **Data 8-15** Bit 2 controls **Data 16-23** Bit 3 controls **Data 24-31**
notVOE	O	This signal connects to the **TRANSFER/OUTPUT ENABLE** of the VRAM. It enables the VRAM outputs at the appropriate times as well as defining serializer load cycles to the VRAM.
VSClkOut	O	This signal causes shift cycles on the VRAM serial ports. The IMS G201 controls the shift timing based on bits per pixel and prescaling of the master clock source from the IMS G191.

22.2.3 IMS G191 interface

Pin name	I/O	Signal description
VideoCtrlOut0-1	O	These pins represent the horizontal scan line state. Table 22.8 (page 502) shows the decoding of the bits.
notDataStrobe2	O	This signal is used to strobe data from the IMS G201 to the IMS G191. It is used to communicate register contents programmed by the host processor and decoded in the IMS G201. A low sent on this pin to the IMS G191 indicates that the IMS G191 should perform the action defined by the **VAddr0-6** and **notRegWE** pins.
CRTClkIn **CRTClkIn2**	I I	CRTC clocks. These clocks are sourced by the IMS G191 and are used by the IMS G201 to generate all video related timings.
MonHSync	O	This is the monitor horizontal sync pulse. It can be programmed to pulse either positive or negative. It enters the high impedance state when **MonSyncOE** is high.
MonVSync	O	This is the monitor vertical sync pulse. It can be programmed to pulse either positive or negative. It enters the high impedance state when **MonSyncOE** is high.
MonSyncOE	I	A low on this input will cause the **MonHSync** and **MonVSync** to three-state their outputs.

22.2.4 Supplies

Pin name	I/O	Signal description
VDD		VDD
GND		GND

22.2.5 Miscellaneous

Pin name	I/O	Signal description
notDataStrobe1	O	This signal strobes low to cause reads and writes to/from the external memory (typically PROM) and external registers.
HoldToGND		Must be connected to **GND**
HoldToVDD		Must be connected to **VDD**
N/C		No Connect (this refers to unused pins). Do not wire this pin.

22.3 Coprocessor

The coprocessor provides hardware drawing assist functions. These functions can be performed on graphics data in both video memory and system memory.

The coprocessor updates memory independent of the system microprocessor. A virtual memory feature allows the coprocessor to perform linear to physical address conversion in a manner consistent with the paging operation in the 80X86 processor family. The instructions are written to a set of memory-mapped registers (see Section 22.7.1); the coprocessor then executes the drawing function.

The coprocessor functions are summarized below:

- Pixel Block Transfer (PxBlt) - This function provides a four term block transfer capability of an entire bit map, or part of a bit map, from one location to another. This transfer can be: within video memory, within system memory, or between system and video memory.
- Line draw - This function draws lines, with a programmable style, into a bit map in video memory or system memory.
- Area fill - This function fills an outlined area with a programmable pattern. It can be performed on an area outline in video or system memory.
- Logical and arithmetic pixel mixes - These functions provide logical and arithmetic operators that can be used against data in video or system memory.
- Scissoring - This function provides a rectangular mask function, which can be used instead of the mask map.
- Map masking - This function provides control over updates to each pixel for all drawing functions.
- X, Y addressing - This function allows a pixel to be specified by its X and Y coordinates within a pixel map, instead of its linear address in memory.
- Virtual addressing - When enabled, this function causes the coprocessor function to utilize a page table of a form identical to the 80X86 processor family page table. A translation look aside buffer is kept on chip to speed conversion of addresses.

22.3.1 Pixels, pixel maps and X, Y addressing

The drawing coprocessor works on pixels within pixel maps. A pixel map is an area of memory at a given address (the base address) with a defined width, height and pixel format. Pixels can have 1, 2, 4, 8 or 16 bits. The pixels can be ordered within bytes in one of two ways: left to right or vice versa. The XGA allows pixel maps of any arbitrary size up to 4096×4096 pixels.

The coprocessor is programmed using X, Y coordinates that are automatically converted into linear memory addresses (using the defined width and pixel size) before accessing the physical memory (see Figure 22.3).

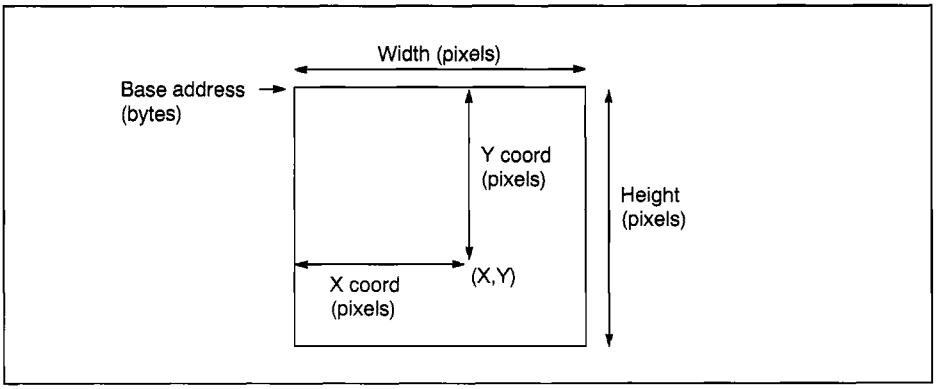

Figure 22.3 Pixels are addressed using X,Y coordinates within pixel maps

The programmer can define up to four pixel maps at one time. Three maps (A, B and C) are general purpose; the other is always used as the mask map. When starting a drawing operation, the programmer tells the coprocessor which maps are to be used as the source, the pattern, and the destination. In this way, map A, for example, could be the display pixel map. It could then be used as source, destination, or both, without having to move the pixel map parameters from one set of registers to another.

22.3.2 Pixel maps in system memory

A certain amount of space is available in the non-displayed (off-screen) areas of video memory. This is often used for storing fonts and off-screen pixel maps. GUIs, however, make extensive use of off-screen pixel maps (for example, for pull-down menus), and may be called upon to use fonts that are too large to fit in off-screen video memory. When the off-screen video memory is full, the GUI device driver can use normal system memory. With previous adapters, this generally meant processing the pixels using the system processor which is slow compared to special drawing hardware, especially if the operation is not a simple copy. It also ties up the processor and prevents it from preparing for the next drawing operation.

The XGA uses bus-mastership on the bus (AT bus or Micro Channel) to overcome these problems. The drawing coprocessor's power can be used on pixel data anywhere in system or video memory.

To support paged memory environments, where the paging unit in the 80386 or 80486 is turned on, the XGA includes its own paging unit, using page tables of the same form. The XGA can operate using the main page tables used by the operating environment (with its cooperation), or on tables built by device drivers or applications themselves.

22.3.3 Pixel block transfer (PxBlt)

The PxBlt function works with four operands: the source, the pattern, the destination and mask. The source may come from a pixel map to copy data, or from color registers to set the destination to a particular color. The pattern may come from a pixel map, indirectly from the source, or it may be disabled.

For each pixel, the source and destination are combined using a Mix function selected by the 1-bit-per-pixel pattern. A 0 in the pattern selects the background mix, and a 1 selects the foreground mix. A full set of logical mixes is provided, supporting OS/2 and Windows Raster Operations (ROPs), with a selection of arithmetic mixes. Fast text drawing is crucial to windowing environments and other interactive applications. The pattern can select between foreground and background colors, allowing a 1-bit-per-pixel text font in the pattern map to be rapidly expanded to colored characters in the destination.

The pattern and the source have another common feature. The X, Y addresses for these maps automatically wrap when they reach either side or top and bottom. This allows a small pattern to be "tiled" over a large area in the destination using a single operation (see Figure 22.4).

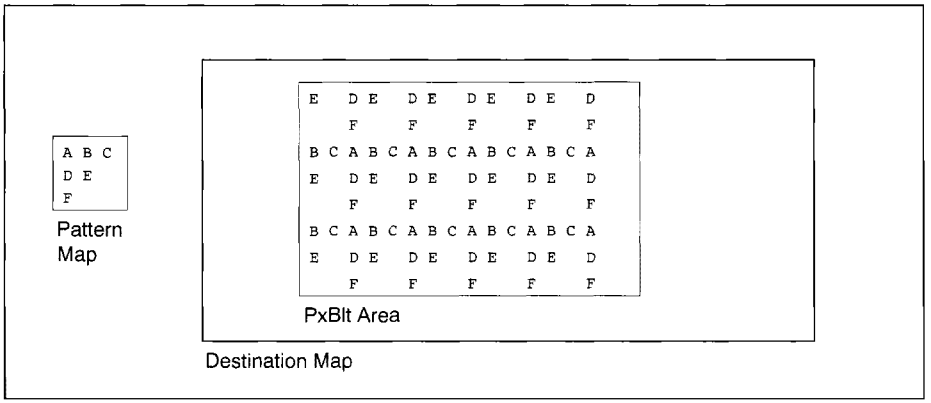

Figure 22.4 Patterns are automatically tiled

22.3.4 Lines

The coprocessor draws lines using the Bresenham line-drawing algorithm. All pixels of a line can be drawn, or the first or last pixel can be suppressed to draw poly lines correctly.

As with PxBlt, the pattern and source X, Y coordinates wrap at the edge of the maps. Line drawing, however, is different. While the X, Y coordinates of the destination move along the required path, the coordinates in the source and pattern move horizontally - left to right only. A simple 1-pixel-high pattern is drawn along the line, as shown in Figure 22.5.

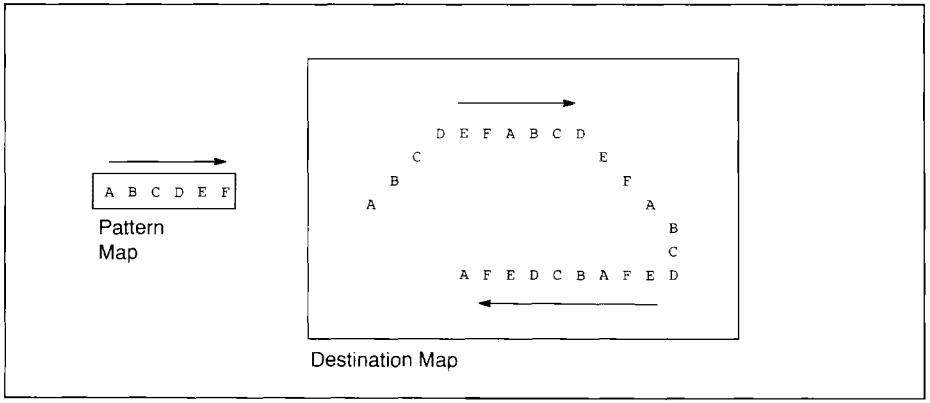

Figure 22.5 Line patterns are also pixel maps

Short lines can be drawn with simpler commands using 'short stroke vectors', line segments up to 16 pixels long, and in one of eight directions (the X axis, the Y axis and the 45° lines in between).

22.3.5 Area fill

The coprocessor allows arbitrary areas to be filled rapidly. The area is defined by an outline drawn in a 1-bit-per-pixel map. The outline is drawn using special versions of the line drawing functions (including short strokes).

When the outline is complete, a special PxBlt fills the inside of the defined figure. A parity fill algorithm is used, where a rectangle is scanned from left to right, starting from outside the figure, and alternately moving in and out of the figure as each successive boundary is crossed. The area can also be filled with a pattern if required.

22.3.6 Scissoring and map masking

The coprocessor can, under programmer control, automatically 'scissor' (that is, not draw) pixels that an operation attempts to draw outside a specified area. That area can be a simple rectangle, or a more complex shape defined in a pixel map (the mask map), with a pattern of 1's and 0's (1 allows the corresponding pixel in the destination to be changed; a 0 protects that pixel). This function can be used, for example, when drawing into a background window that is partially obscured by other windows.

22.3.7 State save and restore

In a multi-tasking environment, the system processor must change tasks from time to time. When changing tasks, the state of the current task must be saved so that it can be restored and continued at a later time. The state of the coprocessor can be rapidly saved and restored, making multi-tasking operation possible.

The coprocessor's operation can be suspended at any time and later resumed. Once suspended, the entire state of the coprocessor, including internal registers not visible in the address space, can be saved to memory by reading repeatedly from two 32 bit I/O ports. The 80X86 string input (INS) instruction can be used for this. The state is restored by writing the previously saved state data back into the same ports (using the OUTS instruction). Once resumed, the operation will continue from exactly the point at which it was suspended.

22.4 System bus interface

This portion of the IMS G201 display controller provides control of the interface between the video subsystem and the system microprocessor. It decodes the addresses for VGA and XGA I/O registers and the memory addresses for the coprocessor memory-mapped registers and video memory. It also provides controls that allow access to: registers in the IMS G191 serializer palette DAC, data in the sprite memory, ROM, and external registers.

The system bus interface is designed to interface to an AT bus or a Micro Channel. For interfacing to an AT bus it supports: both slave and master operations for a 16 bit interface; slave operations only for an 8 bit interface. For interfacing to a Micro Channel it supports both slave and master operations for a 32 bit or a16 bit interface. Refer to Section 22.10.1 detailing the hardware interfaces for further information on the system bus interface.

22.5 CRT and VRAM controller

The memory controller controls accessing of the VRAM. It supports memory either 16 or 32 bits wide. The minimum implementation is 512 Kbytes.

The CRT controller (CRTC) generates all the timing signals required to drive the serializer and the display. It consists of two counters, one for horizontal parameters, and one for vertical parameters, and a series of registers. The counters run continuously, and when the count value reaches that specified in one of the associated registers, the event controlled by that register occurs.

22.5.1 Extended mode CRT controller register interpretations

A pictorial representation of the function of each of the CRT controller registers is shown in Figure 22.6.

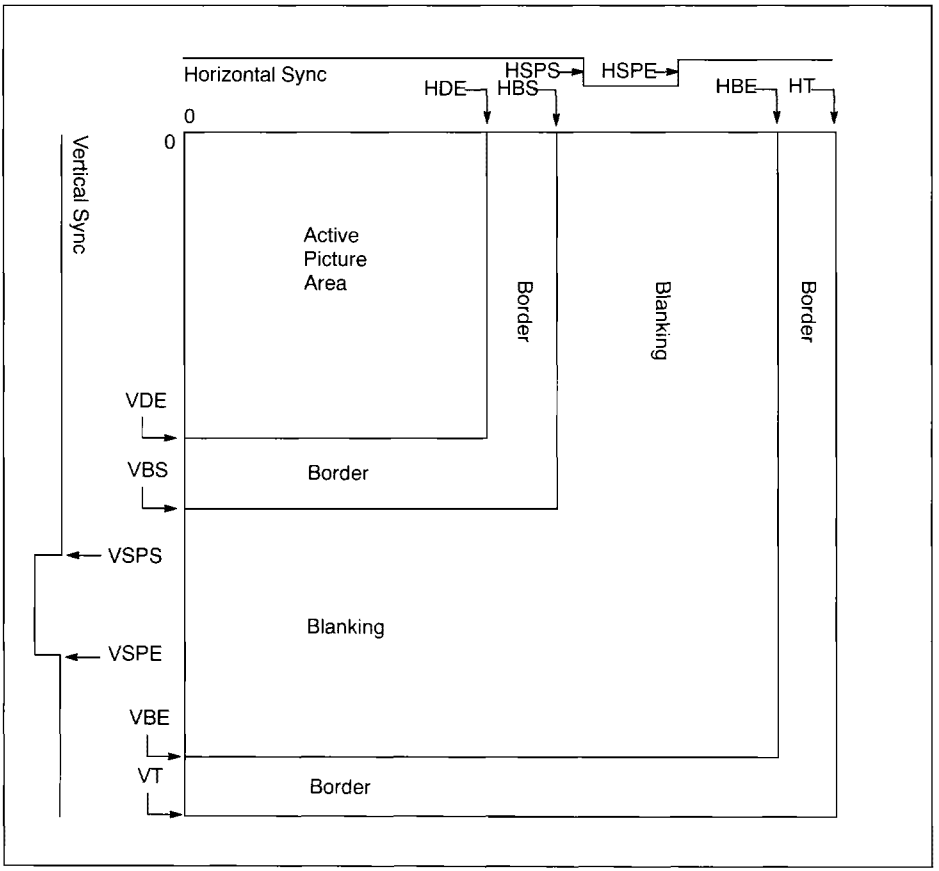

Figure 22.6 CRT controller register definitions

Horizontal scan registers		Vertical scan registers	
HT	Horizontal total register	**VT**	Vertical total register
HDE	Horizontal display end register	**VDE**	Vertical display end register
HBS	Horizontal blanking start register	**VBS**	Vertical blanking start register
HBE	Horizontal blanking end register	**VBE**	Vertical blanking end register
HSPS	Horizontal sync pulse start register	**VSPS**	Vertical sync pulse start register
HSPE	Horizontal sync pulse end register	**VSPE**	Vertical sync pulse end register

Table 22.1 Registers which control a horizontal and a vertical scan of the display

The XGA can be programmed to inform the host processor of the start and the end of the Active Picture Area using a system interrupt. An enable and a status bit exist for each interrupt.

22.6 XGA I/O-mapped and memory-mapped registers

XGA is controlled using a combination of I/O-mapped and memory-mapped registers. I/O-mapped registers are those that appear in the I/O address space of an 80X86 processor, and are accessed using IN, OUT, or other I/O instructions. Memory-mapped registers appear in the memory address space of an 80X86 processor, and are accessed using standard memory operations with all the available combinations of registers and addressing modes. In addition, many I/O-mapped registers are indexed (that is, the register is selected using an index in one I/O port, and the data for all indexed registers is written through a second I/O port). This technique, used also by the VGA, reduces the I/O address space required.

Memory-mapped registers are generally used to control the drawing coprocessor, where frequent access requires good performance. I/O-mapped registers (indexed and direct) are used for the remainder (mainly setup registers, where performance is less important). Table 22.2 shows the XGA direct access I/O registers.

I/O port address	Register	Read/ Write	Description
21x0	Operating mode	R/W	Defines display mode (VGA, 132 or XGA)
21x1	Aperture control	R/W	Controls a 64K aperture through which the XGA memory can be accessed in the system address space. This window gives real mode applications and operating systems a means of accessing the XGA video memory.
21x2			Reserved
21x3			Reserved
21x4	Interrupt enable	R/W	Contains bits to enable/disable the interrupt conditions that can be generated by the subsystem.
21x5	Interrupt status	R/W	Indicates the interrupt status bits that can be generated by the subsystem and used to reset the corresponding interrupts.
21x6	Virtual memory control	R/W	This register is directly mapped to the I/O address space.
21x7	Virtual memory interrupt status	R/W	This register is directly mapped to the I/O address space.
21x8	Aperture index	R/W	Used to provide address bits to the video memory when the aperture in system address space being used is smaller than the amount of video memory installed.
21x9	Memory access mode	R/W	Controls pixel ordering when the video memory is being accessed by the system (not the coprocessor). Intel or Motorola order can be selected. This register also controls the number of bits per pixel.
21xA	Index	R/W	Selects which indexed Extended Graphics Mode register is accessed when any address (base+B) to (base+F) is read or written.
21xB 21xC 21xD 21xE 21xF	Data	R/W	These registers are used when reading and writing to the register indexed by the Index register (21xA). The read/ write operation can be of byte, word, or double-word size using these data registers.

Table 22.2 XGA direct access I/O registers

Multiple XGA adapters (multiple instances) can be used in a system. Each instance has an instance number and has its registers mapped at different addresses. The memory-mapped registers are located at some point within the address range C0000 and DFFFF. The precise location is set by a system dependent configuration process, such as the PS/2 Micro Channel auto-configuration.

It is recommended that instance 0 is not used on AT bus systems, as for some implementations this board number can cause bus conflicts. When using instance 0 on Micro Channel bus systems do not allow the 4MByte video memory aperture to start at address 0xxx, as this will conflict with DOS. Similarly when using instance 7 on MIcro Channel bus systems do not allow the 4MByte video memory aperture to reside at the top of the system address space as this conflicts with some systems' BIOS RAM re-map.

When multiple XGA subsystems are installed in a system, the memory-mapped registers for all instances can be mapped within the same 1 Kbyte block of address space. The allocation of addresses is the responsibility of the system configuration process, which ensures that there is no conflict between installed adapters (XGA or others).

Figure 22.7 illustrates how the I/O registers are located. Base address of the sixteen I/O registers of an XGA is 21x0, where x is the instance number. Figure 22.7 shows instance 6.

Figures 22.8 and 22.9 illustrate how the memory-mapped registers are located for an AT bus and a Micro Channel bus system respectively. These figures show instance 6.

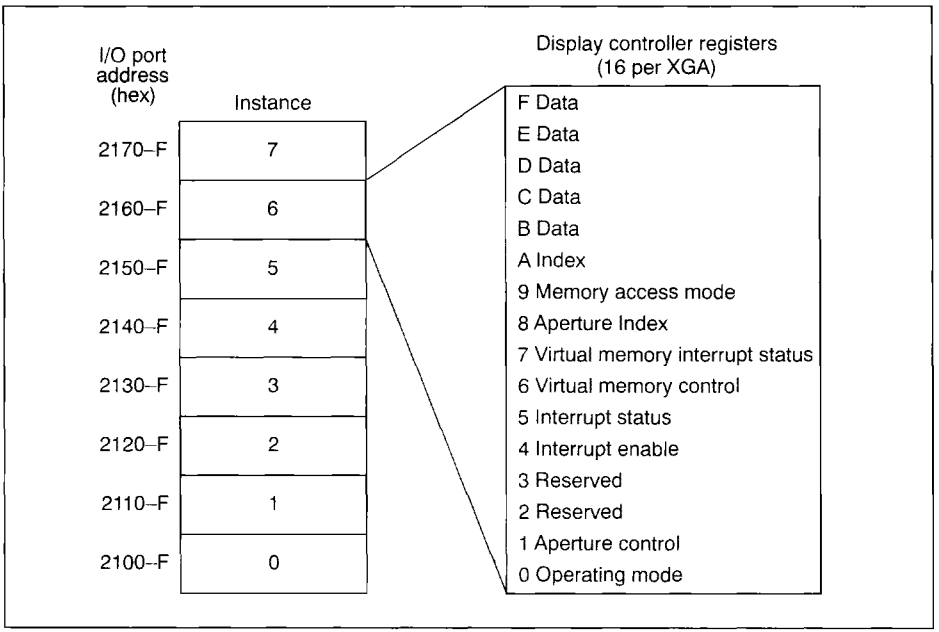

Figure 22.7 I/O port addressing of XGA registers

AT bus system memory-mapped registers

The memory mapped registers occupy 128 bytes of memory in the last 1 Kbyte of a 32 Kbyte address space. This may reside on a 32 Kbyte boundary anywhere between the address range C0000 and DFFFF. The purpose of having a 32 Kbyte region is that the first 31 Kbytes is required for a full BIOS held in the adaptor ROM. The motherboard (planar) implementation of the XGA does not require its own ROM, as the main motherboard ROMs contain all the necessary information, such as XGA initialization code. Adaptor options allow the specification of the BIOS ROM base address and the XGA instance number determines the location of the 128 bytes within the upper 1 Kbyte address space.

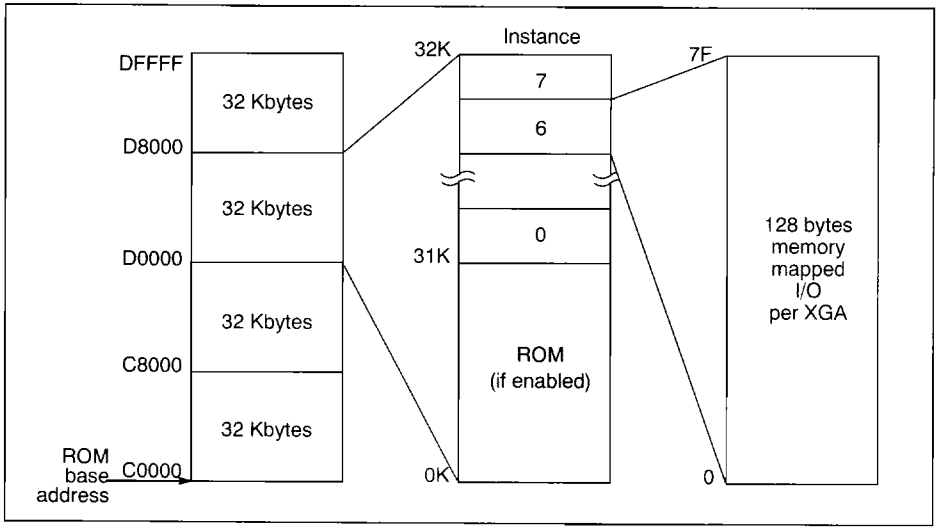

Figure 22.8 Memory mapped addressing of XGA registers for **AT bus** system

Micro Channel system memory-mapped registers

Base address of the memory-mapped registers of an XGA is (ROM Base address) + 7K + (128×instance number). Figure 22.9 shows instance 6.

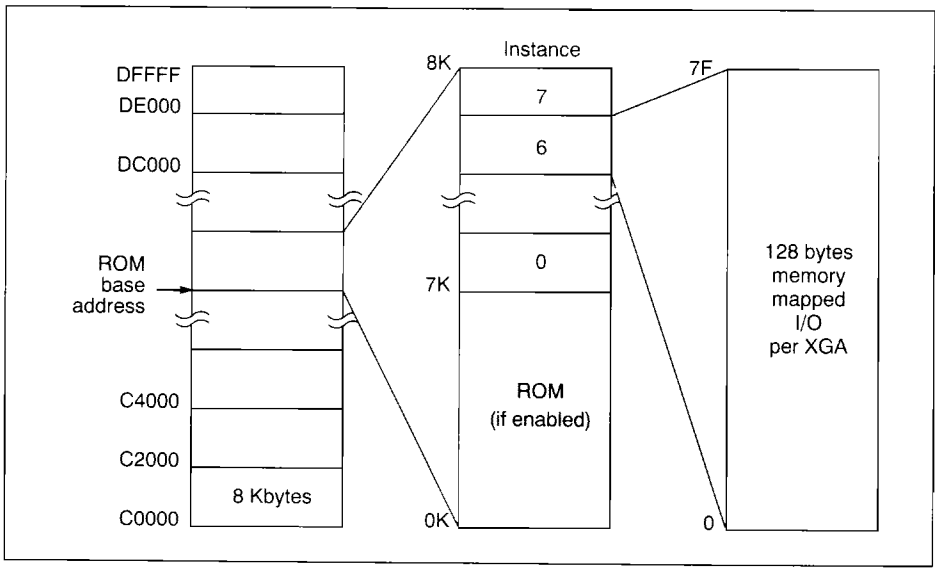

Figure 22.9 Memory mapped addressing of XGA registers for **Micro Channel** system

Traditionally, display adapters such as the VGA and the 8514/A have been controlled through registers mapped into the 80X86 I/O address space. Memory-mapped registers have been introduced in the XGA for controlling the drawing coprocessor, where accesses are frequent and good performance is essential.

The I/O address space in the 80X86 is limited to 64 Kbytes, so individual adapters can only use a restricted number of addresses (to avoid possible conflicts between adapters). When the adapter contains many registers (typical of a display controller), indexed register addressing schemes are often used, as noted above. Memory address space is much larger (1 Mbyte minimum in real mode), so adapters with memory-mapped registers can avoid using indexing, thus allowing direct access to all registers, and reducing code space and execution time.

When the 80386 is running in Protected mode, the processor normally checks I/O accesses by applications to ensure they are allowed. It reads the I/O Permission Bitmap, a process that adds twenty cycles to each individual I/O access. Memory-mapped registers avoid this overhead, reducing to one-tenth the time taken to start many graphics operations.

Another advantage relates to multiple display adapters. Each instance of the XGA has a different set of register addresses, as shown earlier. Software must be able to run with any possible set. The 80X86 allows base-plus-offset addressing for memory accesses, using a segment register and an immediate or register-based offset. The software would typically set the segment register to point to the first address of the memory-mapped registers, and then have immediate pointers to specific registers. I/O addresses, on the other hand, are always contained in the DX register of an 80X86 processor; no form of base-plus-offset addressing is possible. For I/O-mapped registers, DX must be calculated correctly before each access, taking time and code space.

22.7 IMS G201 register reference guide

The following section lists all the IMS G201 registers with a brief description of the function of each register. The complete register bit format is not included in this datasheet, this is defined in the *XGA Software Programmer's Guide*, document number 72 OEK 258 01. All addresses and indexes are in hexadecimal. Unspecified registers, or registers marked as 'RESERVED', are reserved and must not be written to or read from.

22.7.1 IMS G201 memory mapped registers

The IMS G201 coprocessor is controlled using a bank of 128 memory mapped registers. Table 22.3 shows the register memory map for the IMS G201 coprocessor in Intel register format. The register descriptions are given in Table 22.4.

Byte 3	Byte 2	Byte 1	Byte 0	
Page Directory Base Address				0
Current Virtual Address				4
RESERVED		Auxiliary Coprocessor Control	RESERVED	8
RESERVED		State B len	State A len	C
RESERVED	Pixel Map Index	Coprocessor Control	RESERVED	10
Pixel Map n Base Pointer				14
Pixel Map n Height		Pixel Map n Width		18
RESERVED			Pixel Map n Format	1C
RESERVED		Bresenham Error Term		20
RESERVED		Bresenham K1		24
RESERVED		Bresenham K2		28
Direction Steps				2C
RESERVED				30
RESERVED				34
RESERVED				38
RESERVED				3C
RESERVED				40
RESERVED				44
RESERVED	Dest Color Comp. Cond.	Bgd Mix	Fgd Mix	48
Destination Color Compare Value				4C
Pixel Bit Mask				50
Carry Chain Mask				54
Foreground Color Register				58
Background Color Register				5C
Operation Dimension 2		Operation Dimension 1		60
RESERVED				64
RESERVED				68
Mask Map Origin Y Offset		Mask Map Origin X Offset		6C
Source Map Y Adr		Source Map X Adr		70
Pattern Map Y Adr		Pattern Map X Adr		74
Dest. Map Y Adr		Dest. Map X Adr		78
Pixel Operation				7C

Table 22.3 IMS G201 coprocessor register memory map (Intel format)

Off-set	Register	Read/ Write	Description
0	Page Directory Base Address	Write	Contains a 20 bit pointer to the page in physical memory containing the current Page Directory for the current task.
4	Current Virtual Address	Read	Contains the faulting page address in the event of a 'Not Present' or 'Protection Interrupt' being flagged.
9	Auxiliary Coprocessor Control	Read	Contains a duplicate status bit to the Coprocessor Busy bit (BSy, bit 7) of the Coprocessor Control register. The state of this bit is provided on the **CoProcStat** pin, enabling the busy status to be read without halting the coprocessor.
C D	State A len State B len	Read	These registers return the length, in double words, of the two parts, A and B of the coprocessor state for save and restore.
11	Coprocessor Control	R/W	Indicates if the coprocessor is currently executing an operation. In addition, the current coprocessor operation can be terminated or suspended by writing to this register.
12	Pixel Map Index	Write	Selects which of the pixel maps (A, B, C or mask) the four pixel map description registers apply.
14	Pixel Map n Base Pointer	Write	Specifies the byte address in memory of the start of a pixel map. If virtual address mode is enabled this address is a virtual address, otherwise it is a physical address.
18	Pixel Map n Width	Write	Specifies the width in pixels of a pixel map.
1A	Pixel Map n Height	Write	Specifies the height in pixels of a pixel map.
1C	Pixel Map n Format	Write	Specifies the format of a pixel map (Intel or Motorola) and the size of a pixel map in bits/pixel.
20	Bresenham Error Term	R/W	Specifies the Bresenham Error Term (E) for the draw line function.
24	Bresenham K1	Write	Specifies the Bresenham Constant (K1) for the draw line function.
28	Bresenham K2	Write	Specifies the Bresenham Constant (K2) for the draw line function.
2C	Direction Steps	Write	Used to specify up to 4 draw and step codes to the coprocessor and to initiate a draw and step operation.
48	Fgd Mix	Write	Holds the foreground mix value that specifies a logic or arithmetic function to be performed between the Destination and Function 1 second operand pixels during an operation where the Pattern pixel value is 1.
49	Bgd Mix	Write	Holds the background mix value that specifies a logic or arithmetic function to be performed between the Destination and Function 0 second operand pixels during an operation where the Pattern pixel value is 0.
4A	Dest Color Comp. Cond.	Write	Specifies the destination color compare condition under which destination update is inhibited.
4C	Destination Color Compare Value	Write	Contains the comparison value with which the destination pixels are compared when color compare is enabled.
50	Pixel Bit Mask	Write	Specifies which bits within each pixel are to be updated by the coprocessor.

Off-set	Register	Read/ Write	Description
54	Carry Chain Mask	Write	Contains a mask up to 31 bits wide. The mask is used to specify how the carry chain of the ALU is propagated when performing arithmetic update mixes and color compare operations.
58	Foreground Color Register	Write	Holds the foreground color to be used during coprocessor operations. The foreground color can be specified as the Foreground Source by setting up the appropriate field in the Pixel Operation Register.
5C	Background Color Register	Write	Holds the background color to be used during coprocessor operations. The background color can be specified as the Background Source by setting up the appropriate field in the Pixel Operation Register.
60	Operation Dimension 1	Write	Specifies the width of the rectangle to be drawn by the PxBlt function, or the length of the line in a line draw operation.
62	Operation Dimension 2	Write	Specifies the height of the rectangle to be drawn by the PxBlt function.
6C 6C	Mask Map Origin X Offset Mask Map Origin Y Offset	Write	These registers specify the X and Y offset of the Mask Map origin relative to the origin of the Destination Map.
70 72	Source Map X Adr Source Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Source pixel.
74 76	Pattern Map X Adr Pattern Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Pattern pixel.
78 7A	Dest. Map X Adr Dest. Map Y Adr	R/W	These registers specify the X and Y coordinates of the coprocessor operation Destination pixel.
7C	Pixel Operation	Write	It is used to define the flow of data during an operation, specifies the address update function that is to be performed, and initiates PxBlt and Line Draw operations.

Table 22.4 IMS G201 coprocessor memory mapped register descriptions

22.7.2 IMS G201 XGA indexed access I/O registers

The following table lists all the XGA indexed access I/O registers. Where a G191 address is given, the register does not reside in the IMS G201, but resides in the IMS G191. The IMS G201 delivers an address to the IMS G191 to access the register. Where no G191 address is given the register resides in the IMS G201.

There are four registers which are shared by the IMS G201 and the IMS G191 (index 30, 50, 51 and 54). These registers reside in both chips.

G201 Index	G191 Addr.	Register		Read/ Write	Description
00 01 02	01	Memory configuration 0 Memory configuration 1 Memory configuration 2			These registers are card design specific and are used to configure the chip. They will vary depending on the amount and type of VRAM used.
03					RESERVED
04 05		Auto-configuration 1 Auto-configuration 2		Read	See Section 22.9 for a description of each register.
06-0B					RESERVED
0C 0D		Coprocessor save/restore	data A data B		These registers are an image of a port in the coprocessor. They are used to save and restore the two parts, A and B, of the internal state of the coprocessor.
0E-0F					RESERVED
10 11		Horizontal total	Lo Hi	R/W	These registers define the total length of a scan line in units of eight pixels.
12 13		Horizontal display end	Lo Hi	R/W	These registers define the position of the end of the active picture area relative to (after) the start of the active picture area in units of eight pixels.
14 15		Horizontal blanking start	Lo Hi	R/W	These registers define the position of the end of the picture border area relative to (after) the start of the active picture area in units of eight pixels.
16 17		Horizontal blanking end	Lo Hi	R/W	These registers define the position of the start of the picture border area relative to (after) the start of the active picture area in units of eight pixels.
18 19		Horizontal sync pulse start	Lo Hi	R/W	These registers define the position of the start of horizontal sync pulse relative to (after) the start of the active picture area in units of eight pixels.
1A 1B		Horizontal sync pulse end	Lo Hi	R/W	These registers define the position of the end of horizontal sync pulse relative to (after) the start of the active picture area in units of eight pixels. This Extended Graphics Mode register is also used in 132 Column Text Mode in place of the VGA 'End Horizontal Retrace' register. In that mode each eight pixel unit is equivalent to one character.

G201 Index	G191 Addr.	Register		Read/ Write	Description
1C 1Er		Horizontal sync position		Write	These registers allow the HSYNC signal to be delayed by up to 6 pixels. The required value **must** be written to both registers. Note that for a delay of four pixels this value is zero.
1D					RESERVED
1F					RESERVED
20 21		Vertical total	Lo Hi	R/W	These registers define the total length of a **frame** in units of one scan line.
22 23		Vertical display end enable	Lo Hi	R/W	These registers define the position of the end of the active picture area relative to (after) the start of the active picture area in one scan line units.
24 25		Vertical blanking start	Lo Hi	R/W	These registers define the position of the end of the picture border area relative to (after) the start of the active picture area in units of one scan line.
26 27		Vertical blanking end	Lo Hi	R/W	These registers define the position of the start of the picture border area relative to (after) the start of the active picture area in units of one scan line.
28 29		Vertical sync pulse start	Lo Hi	R/W	These registers define the position of the start of the vertical sync pulse relative to (after) the start of the active picture area in units of one scan line.
2A		Vertical sync pulse end		R/W	This register defines the position of the end of vertical sync pulse. The value loaded is the Least Significant (LS) byte of a 16 bit value which defines the end of the vertical sync pulse relative to (after) the start of the active picture area in units of one scan line. The vertical sync end position **must** be within 31 scan lines of the vertical sync start position.
2B					RESERVED
2C 2D		Vertical line compare	Lo Hi	R/W	These registers define the position of the end of the scrollable picture area relative to (after) the start of the active picture area in units of one scan line.
2E-2F					RESERVED
30* 31	03	Sprite horizontal start	Lo Hi	R/W	These registers define the position of the start of the Sprite relative to (after) the start of the active picture area in pixels.
32	04	Sprite horizontal preset		R/W	This register resides in the IMS G191.
33 34		Sprite vertical start	Lo Hi	R/W	These registers define the position of the start of the Sprite relative to (after) the start of the active picture area in units of one scan line.

G201 Index	G191 Addr.	Register	Read/ Write	Description
35		Sprite vertical preset	R/W	This register defines the vertical position within the 64 by 64 sprite area at which the Sprite starts. The sprite always ends at position 63 (i.e. it does not wrap).
36	05	Sprite control	R/W	This register resides in the IMS G191.
37				RESERVED
38 39 3A 3B 3C 3D	38 39 3A 3B 3C 3D	Sprite color 0 red Sprite color 0 green Sprite color 0 blue Sprite color 1 red Sprite color 1 green Sprite color 1 blue	R/W	These registers reside in the IMS G191.
3E-3F				RESERVED
40 41 42		Start address Lo Start address Mi Start address Hi	R/W	These registers define the address of the start of the visible portion of the video buffer in units of 8 bytes.
43 44		Buffer pitch Lo Buffer pitch Hi	R/W	These registers define the amount of memory allocated for each scan line in units of 8 bytes.
45-4F				RESERVED
50*	06	Display Mode 1	R/W	This register contains fields defining the display blanking, display scan order, video extension enabled /disabled, and sync polarity.
51*	07	Display mode 2	R/W	This register contains fields defining the pixel size (for the serializer, palette and DAC) and the display scale factors (horizontal and vertical).
52	08	Display ID and comparator	Read	This register contains fields indicating the type of display attached and the state of three diagnostic status bits associated with the DAC.
53	09	System ID	Read	The contents of this register return the display controller ID.
54*	0A	Clock frequency select 1	R/W	Selects the IMS G191 clock scale factor and the register used to program the pixel clock.
55	0B	Border color	R/W	This register holds the Border Color palette index.
56*	0C	Fixed clock frequency address	R/W	Used to address the Fixed pixel clock frequency registers.
57*	0D	Fixed clock frequency data	R/W	Provides access to the Fixed pixel clock frequency registers.
58*	0E	Programmed pixel clock frequency	R/W	Can be programmed to contain a frequency value for the IMS G191 PLL.
59-5A				RESERVED
5B*	1D	Miscellaneous control 1		Controls a number of IMS G191 functions.
5C-5F				RESERVED

G201 Index	G191 Addr.	Register	Read/ Write	Description
60 61	10 11	Sprite/palette index Lo Sprite index Hi	R/W	These registers are used for specifying the index when reading from the Sprite or the Palette, with subsequent incrementing of the index.
62 63	12 13	Sprite/palette index with prefetch Lo Sprite index with prefetch Hi	R/W	These registers are used for specifying the index when reading from the Sprite or the Palette.
64	14	Palette mask	R/W	The contents of this register are ANDed with each Display Memory Pixel Value and the result is used to index the palette.
65	15	Palette data	R/W	This register contains an image of the currently selected Palette RAM location.
66	16	Palette sequence	R/W	This register contains two fields, one defining which of the R,G or B elements of the currently selected palette location is the current one for the Palette data register, the other defining the sequence to be followed for selecting the R,G and B elements for successive Palette Data Register accesses.
67 68 69	17 18 19	Palette red prefetch Palette green prefetch Palette blue prefetch	R/W	These registers are not used for any normal function but **must** be saved and subsequently restored by any interrupting code that uses the sprite or palette registers.
6A	1A	Sprite data	R/W	This register is an image of the currently selected Sprite buffer location.
6B	1B	Sprite prefetch register	R/W	This register is not used for any normal function but **must** be saved and subsequently restored by any interrupting code that uses the sprite or palette registers.
6C*	1E	Miscellaneous control 2		Controls blanking of red and blue DACs.
6D-6F	1F–3F			RESERVED
70*	37	Clock frequency select 2	R/W	Used in conjunction with the Clock frequency select 1 register.
71		ROM paging		The contents of this register allow the 8/32K ROM space to be paged.
72-7F				RESERVED

Note: A * denotes that this register is shared by the IMS G201 and IMS G191.

Table 22.5 Indexed I/O register descriptions

22.7.3 IMS G201 VGA indexed access I/O registers

The IMS G201 contains all the VGA registers (as defined in the 'Video subsystem' section in the *IBM Video Technical Reference*, document number 42G2193), with the exception of those registers or register bits listed below which are in the IMS G191. For a complete list of those VGA registers which reside in the IMS G191 refer to the *IMS G191 XGA serializer palette DAC datasheet*, document number 42 1526 02.

VGA Address		IMS G191 VGA Index	Bits not in IMS G201	Register name
Wr @	Rd @			
3C0	3C1	N/A	5	Attribute address
3C0	3C1	3C0=0-0F	All bits	Internal palette
3C0	3C1	3C0=10	All bits	Attribute mode control
3C0	3C1	3C0=11	All bits	Attribute overscan color
3C0	3C1	3C0=12	All bits	Attribute color plane enable
3C0	3C1	3C0=13	All bits	Attribute horizontal pixel pan
3C0	3C1	3C0=14	All bits	Attribute color select
3C2	3CC	N/A	2,3	Miscellaneous output
N/A	3C2	N/A	4	Input status zero
3C5	3C5	3C4=00	All bits	Sequencer reset
3C5	3C5	3C4=01	All bits	Sequencer clocking mode
3CF	3CF	3CE=05	5,6	Graphics mode
3C6	3C6	N/A	All bits	Palette mask
3C7	3C7	N/A	All bits	Palette pixel address (Rd)/ DAC state
3C8	3C8	N/A	All bits	Palette pixel address (Wr)
3C9	3C9	N/A	All bits	Palette data

Note: 'All bits' refers to all bits defined in the *IBM PS/2 Hardware Interface Technical Reference*.

22.8 IMS G201 / IMS G191 communication

22.8.1 IMS G191 register accesses

Because the bus interface function is implemented by the IMS G201 display controller, all updates to registers physically resident in the IMS G191 are decoded by the IMS G201 which then updates the IMS G191. Data for these registers is transferred over the **Data0-7** pins; the address being generated by the IMS G201 **VAddr0-6** pins driving IMS G191 **RegAddr0-6**.

Parameter register accesses are timed by the IMS G201 controller clock (**Clk**), which results in a clock period of 50ns (with the controller operating at 40MHz). A parameter register access occurs whenever **notDataStrobe** is active and address bit 6 is '0'.

There are two basic types of accesses between the IMS G201 and IMS G191, fast accesses and slow accesses. Fast accesses are used for parameter register updates to the IMS G191 and slow accesses are used for sprite/palette accesses since extra time is needed to allow the sprite buffer or the palette RAM to be accessed.

22.8.2 Control codes from the IMS G201 to the IMS G191

The address bits on the IMS G201/IMS G191 interface are used at certain times to carry control data from the IMS G201 to the IMS G191. This data is not transferred as a result of bus activity, but during each VRAM transfer cycle, in particular during the transfer cycle at the start of each line. This data mainly consists of information about the line that is about to be displayed. The data is not transferred on the data bus, but on the low-order six bits of the address.

These bits are encoded as shown in Table 22.6 with their usage described in Table 22.7.

RegAddr0-6							IMS G191 decoded meaning
6	5	4	3	2	1	0	
0	@	@	@	@	@	@	IMS G191 parameter register address
1	0	N	A	S	U	C	control code
1	1	R	R	R	R	R	control code

Table 22.6 Encoding of register address bits 0-6

Symbol	Register address bit usage
@	Address bits used to address the parameter registers within the IMS G191
N	The 'new font pair' bit. When this bit is '1' it causes a reset of the sprite buffer address register used during alphanumeric font loading.
A	The 'active line' bit. This bit is '1' for picture lines, and '0' for border (overscan) lines and for blank (flyback) lines.
S	The 'scrollable/border line' bit. When it is '1' during an active line it indicates that the line is scrollable. When it is '1' during a non-active line it indicates that the line is a border line.
U	The 'underline/panning sync/sprite line' bit. In an alphanumeric VGA mode it is '1' to indicate that the underline part of a character should be placed on the line. In extended mode it is '1' to indicate that the sprite should be placed on the line. In addition, if this bit is '1' during a non-active line, it causes the horizontal panning sync register to be strobed.
R	In VGA mode these bits are character row bits 4:0. In extended mode these bits hold the sprite prefetch row number, indicating in which row the sprite is to be displayed.
C	C is bit 5 of the sprite row number.

Table 22.7 Register address bit usage

22.8.3 Video control

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G201 from the IMS G191 CRTC clocks and fed back into the IMS G191 via the **VideoCtrlIn0-1** pins. The video control signals are encoded as shown in Table 22.8 to indicate events on a horizontal scan line.

VideoCtrlOut0-1		Video data function
Bit 1	Bit 0	
0	0	Blanking
0	1	Border
1	0	Picture
1	1	Picture and start of cursor

Table 22.8 **VideoCtrlOut0-1** decoding

22.9 IMS G201 device configuration

The devices in the XGA chipset can be configured by a combination of auto-configuration and values written to the Programmable Option Select (POS) registers. In addition the local memory resident in the XGA subsystem can be configured by writing values to the memory configuration registers.

22.9.1 Reset and Initialization

On reset and during initialization the IMS G201 performs an auto configuration cycle. This is an automatic procedure which occurs during **Reset**. During this cycle **notDataStrobe1** and **Data27** will pulse low to allow external buffers to decode the auto-configuration values onto the required data lines. This is the only time that both of these pins will pulse low together, see Figure 22.10. Reset timings are given in Section 22.12.9, page 556.

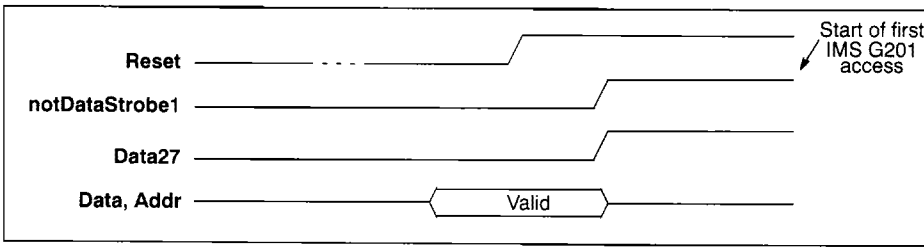

Figure 22.10 Reset sequence

The following pseudo-code describes the initialization process that is executed by the IMS G201 after a reset. This pseudo-code represents the process followed for AT bus and Micro Channel implementations.

```
BEGIN Power On Reset
     Load AutoConfig Registers 1 & 2 from data bus
         IF (Micro Channel)
                 Configure interface for Micro Channel
                 IF (32 bit interface)
                         Configure for 32 bit Micro Channel interface
                 ELSE
                         Configure for 16 bit Micro Channel interface
                 ENDIF
         ELSE
                 Configure interface and POS registers for AT bus
                 Load POS Registers 102, 103, & 105 from address bus
                 IF (Adaptor Implementation)
                         Enable Port #96 emulation
                 ENDIF
                 IF (16 bit interface)
                         Configure interface for 16 bits
                 ELSE
                         Configure interface for 8 bits
                         Disallow bus mastership
                 ENDIF
         ENDIF
 END
```

22.9.2 IMS G201 AT bus configuration

Auto configuration register loading

G201 Index	Register	Read/ Write
04 05	Auto-configuration 1 Auto-configuration 2	Read

The auto-configuration registers 1 and 2 (XGA indexes 4 and 5) are loaded from the IMS G201 data bus during reset. Auto-configuration load data should be gated onto the data bus when **Data27** and **notDataStrobe1** are both low. The following table shows which data bits are loaded into which auto-configuration register fields.

Data bits	Auto-config register	Definition
Data0, Data3	1 (index 4) bits 0 & 3	Data bus size bits 0 & 1
Data1, Data2	1 (index 4) bits 1–2	POS ID bits 0 & 1
Data4	1 (index 4) bit 4	Bus (AT bus or Micro Channel)
Data8–10	2 (index 5) bits 0–2	AT bus adaptor number
Data12	2 (index 5) bit 4	Motherboard/Adaptor sense bit
Data13–15	2 (index 5) bits 5–7	Sense switches (used to read DMA channel selection for AT bus adaptors)

Auto configuration register 1 (Index: #04)

7	6	5	4	3	2	1	0
0	0	0	BF	BS1	POS ID		BS0

Bit name	Definition
BS0–1	These bits indicate the physical size of the system data bus. **Bus size BS1:0** / **Physical bus width** 0 0 — 16 bits 0 1 — 32 bits 1 0 — 8 bits 1 1 — Reserved
POS ID	These bits provide the four extensions to the 16 bit POS ID value read from POS 0 and POS 1 when setup mode is enabled.
BF	This bit indicates, for which bus the IMS G201 system interface is configured. A logic 1 indicates AT bus and a 0 indicates Micro Channel.

Auto configuration register 2 (Index: #05)

7	6	5	4	3	2	1	0
Sense switches			P	0	Adaptor number		

Bit name	Definition
Adaptor number	These bits indicate the AT bus Adaptor number 0–7.
P	When this bit is 1 the IMS G201 is implemented on the motherboard. When 0 the device is on an adaptor.
Sense switches	These sense switch bits are provided to reflect the state of external card level switches loaded during the AT bus auto configuration cycle. These bits are not used by the IMS G201 but are provided as a service to configuration software.

IMS G201 AT bus POS registers

XGA software uses programmable options to determine the location of the I/O and coprocessor registers, and the availability of the memory apertures. The registers which hold these options are called the Programmable Option Select registers.

Auto POS registers loading

The IMS G201 supports the automatic loading of POS register information in addition to auto configuration register loading. The auto POS register data is gated onto the address bus when **Data27** and **notDataStrobe1** are both low. The following table shows which address bits are loaded into which POS register fields.

Address bit	POS register bit locations loaded	Definition
Addr1– 3	Register #102 bits 1–3	I/O Device Address
Addr6–7	Register #102 bits 6–7	External memory address
Addr8	Register #103 bit 0	Enable 8 bit I/O
Addr9	Register #103 bit 1	Enable external memory
Addr10	Register #103 bit 2	Enable 16 bit VGA aperture
Addr13–14	Register #103 bits 5–6	Pacing control
Addr15	Register #103 bits 5–7	Preempt control
Addr16–19	Register #105 bits 0–3	1M byte aperture address
UnLatAddr20	Register #105 bit 4	16 bit coprocessor registers
UnLatAddr21	Register #105 bit 5	Enable shadow registers

Adaptor POS control register: (I/O port #96)

7	6	5	4	3	2	1	0
0	0	0	0	S	Adaptor number		

Bit name	Definition
Adaptor number	These three bits are binary coded slot number values between 0 and 7.
S	This is the setup enable bit which is high to enable setup mode and low to disable.

In AT bus mode the IMS G201 implements I/O port #96 as a write only adaptor setup register. The IMS G201 monitors writes to I/O port #96, comparing the adaptor's setup register bits 0–2, to determine if it is to respond to POS register accesses at I/O ports #0100-#0107.

Adaptor Auxiliary POS control registers: (I/O port #0108+adaptor number)

7	6	5	4	3	2	1	0
0	0	0	0	S	Adaptor number		

Bit name	Definition
Adaptor number	These three bits are binary coded slot number values between 0 and 7.

Adaptor number	Read and write access
0	Read/write I/O port #0108
1	Read/write I/O port #0109
2	Read/write I/O port #010A
3	Read/write I/O port #010B
4	Read/write I/O port #010C
5	Read/write I/O port #010D
6	Read/write I/O port #010E
7	Read/write I/O port #010F

S	This is the setup enable bit which is high to enable setup mode and low to disable.

To provide read and write access to the POS control registers the IMS G201 additionally decodes I/O addresses #0108-#010F. One address for each of the eight possible card numbers then allows 'card exclusive' read and write POS register access via the mirrored port at #96.

The following section describes the IMS G201 POS register bit allocations in AT bus mode. The setup mode is enabled when the unique card number sampled during the auto configuration cycle is compared to the adaptor's setup register bits 0–2 in the I/O ports at either #96 or (#0108+card number) and bit 3 is written to logic 1.

POS Register 0: (Setup mode enabled and I/O address #0100)

7	6	5	4	3	2	1	0
1	1	0	1	1	0	ID option	

This read only register provides the XGA POS identification low byte, returning the value #DB + ID option.

POS Register 1: (Setup mode enabled and I/O address #0101)

This read only register provides the XGA POS identification high byte. The value returned is #8F.

POS Register 2: (Setup mode enabled and I/O address #0102)

7	6	5	4	3	2	1	0
External Memory Addr				IODA			XGA En

Bit name	Definition
XGA En (XGA Enable)	When set to 1 identifies that the subsystem is enabled for address decoding for all non POS addresses. When 0, only POS registers can be accessed, all other accesses to the subsystem have no effect.
IODA (I/O Device Address)	This field specifies which set of I/O addresses has been allocated to the IMS G201 registers, i.e. the instance number (refer to Figure 22.7, page 490).
External Memory Address	These four bits control the addressing of the G201 external memory decode. Only bits 6 and 7 are used. They specify which of four possible 32 Kbyte memory blocks has been assigned to the XGA external memory. The external memory occupies the first 31 Kbytes of this 32 Kbytes block, the other 1 Kbyte being occupied by the coprocessor memory-mapped registers, up to 8 instances each occupying 128 bytes (see Figure 22.8, page 491). Bits 4 and 5 are forced to '11'b to ensure that applications and drivers correctly locate the coprocessor registers in the top 1 Kbytes of the upper 8 Kbytes of the 32 Kbyte ROM space.

POS Register 3: (Setup mode enabled and I/O address #0103)

7	6	5	4	3	2	1	0
Pre empt	Pacing Control		DMA channel		16bit VGA	EM En	8bit I/O

Bit name	Definition
8bit I/O enable	When this bit is 1, all G201 I/O operations are 8 bit. When 1 all I/O operations are 16 bit. This provides a solution for timing problems with 16 bit I/O that exist in systems such as the IBM Model 30-286. It also allows systems that have a conflict with VGA register 3C3h to be programmed to 8 bit I/O thus avoiding the problem caused by device drivers that write to this reserved register.
EM	External Memory is enabled for address decoding when this bit is 1. When set to 0 external memory decoding is disabled. In a multiple instance XGA system in the AT-bus environment one adaptor must be defined as the *primary adaptor*. Only the primary adaptor will have it's Video BIOS ROM enabled, with all other adaptors in the system being serviced from the primary.
16bit VGA memory block	When this bit location is 1 the IMS G201 will respond as a 16 bit memory device for any memory access within the 0A0000–0BFFFF video memory block, regardless of the actual video buffer size. The AT bus specification requires that the –MEMCS16 signal be a decode of the unlatched address signals LA17–LA23, which limits the granularity of this signal to 128Kbytes. To disable 16bit memory cycles this bit must be written to 0.
DMA channel	These bits define up to three AT bus DMA channels and a no-DMA condition as described below. The IMS G201 will power up in the no-DMA condition. If the IMS G201 based XGA subsystem is plugged into an 8 bit slot, then these bits are read only and bus mastership is disabled.

DMA channel bits		DMA assignment
0	0	No DMA
0	1	DMA channel 5
1	0	DMA channel 6
1	1	DMA channel 7

Pacing control	These bits define how much time alternate bus masters and DMA devices are allowed to use within a 100µs period. The intent of the pacing control is to guarantee a minimum amount of CPU performance.

Pacing control bits		Maximum master/DMA time (µs)
0	0	50
0	1	70
1	0	82
1	1	90

Preempt control	This bit determines how long the IMS G201 will hold the bus after it detects a preempt condition. When the bit is 0 the IMS G201 will get off the bus when the current cycle has completed. When the bit is 1, it will wait 4µs before getting off.

POS Register 4: (Setup mode enabled and I/O address #0104 for AT bus Adaptor)

7	6	5	4	3	2	1	0
Video Memory Base							VE

Bit name	Definition
VE (Video memory enable)	This bit signifies whether the 4Mbyte aperture is available for use. In the AT-bus environment this bit is always set to 0.
Video Memory Base Address	This register contains the most significant 7 bits of the address at which the XGA external memory is located. Three more bits are provided by the I/O Device Address in POS register 2. This gives a Video Memory Base address on a 4Mbyte boundary above 32 Mbytes. This field powers up to '0000001'b in the AT bus mode.

POS Register 5: (Setup mode enabled and I/O address #0105)

7	6	5	4	3	2	1	0
0	0	Reg En	16bit copr	1Mbyte Base			

Bit name	Definition
1Mbyte Base	This field specifies where the 1Mbyte aperture has been positioned in the system address space, in increments of Mbytes. A '0000'b in the field will disable the aperture. A '1111'b in this field will also disable the aperture to avoid collisions with the system ROM residing in the last 128 Kbytes of the aperture at #F00000–#FFFFFF.
16bit Coprocessor Registers	This bit configures the G201 for 8 bit or 16 bit memory operations to the memory-mapped Coprocessor registers and the ROM address space. A 1 selects 16 bit memory and 0 selects 8 bit memory. This bit should be set to 0 if there are 8 bit ROMs located in the 128K adaptor ROM area.
Enable shadow registers	When set to 1 this bit will enable the Coprocessor shadow registers.

22.9.3 IMS G201 Micro Channel configuration

Auto configuration registers

G201 Index	G191 Addr.	Register	Read/ Write
04 05		Auto-configuration 1 Auto-configuration 2	Read

The auto-configuration registers 1 and 2 (XGA CRTC indexes 4 and 5) are loaded from the IMS G201 data bus during a reset. Auto-configuration load data should be gated onto the data bus when **Data27** and **not-DataStrobe1** are both low. The following table shows which data bits are loaded into which Auto-Config register fields. The Auto-Config Registers are described in the XGA native registers section of this document.

Data bits	Auto-config register	Definition
Data0, Data3	1 (index 4) bits 0 & 3	Data bus size bits 0 & 1
Data1, Data2	1 (index 4) bits 1–2	POS ID bits 0 & 1
Data4	1 (index 4) bit 4	Bus (AT bus or Micro Channel)
Data8–10	2 (index 5) bits 0–2	AT bus adaptor number
Data12	2 (index 5) bit 4	Motherboard/Adaptor sense bit
Data13–15	2 (index 5) bits 5–7	Sense switches (used to read DMA channel selection for AT bus adaptors)

Auto configuration register 1 (Index: #04)

7	6	5	4	3	2	1	0
0	0	0	BF	BS1	POS ID		BS0

Bit name	Definition
BS0–1	These bits indicate the physical size of the system data bus. **Bus size BS1:0** / **Physical bus width** 0 0 — 16 bits 0 1 — 32 bits 1 0 — 8 bits 1 1 — Reserved
POS ID	These bits provide the four extensions to the 16 bit POS ID value read from POS 0 and POS 1 when setup mode is enabled.
BF	This bit indicates, for which bus the IMS G201 system interface is configured. A logic 1 indicates AT bus and a 0 indicates Micro Channel.

Auto configuration register 2 (Index: #05)

7	6	5	4	3	2	1	0
Sense switches			P	0	0	0	0

Bit name	Definition
P	When this bit is 1 the IMS G201 is implemented on the motherboard. When 0 the device is on an adaptor.
Sense switches	These sense switch bits are provided to reflect the state of external card level switches loaded during the Micro Channel auto configuration cycle. These bits are not used by the IMS G201 but are provided as a service to configuration software.

IMS G201 Micro Channel POS registers

XGA software uses programmable options to determine the location of the I/O and coprocessor registers, and the availability of the memory apertures. The registers which hold these options are called the Programmable Option Select registers.

All Micro Channel compatible adaptors are configured by programming each card's configuration I/O locations at power on, in the power-on self-test (POST) sequence. In order to implement this programmable configuration, I/O addresses #0100–#0107 are defined as the Programmable Option Select (POS) registers which are accessible when the **notSetup** pin on the IMS G201 is active during an I/O cycle. The POS register address is specified on **Addr0–2**; **Addr3–15** are ignored. This requires that the external device (eg. the motherboard) performs a high level decode on I/O address signals **Addr3–15** and drives **notSetup** low only for valid POS addresses.

In Micro Channel systems I/O port #96 controls the **notSetup** signal for each card slot. Only one card can be in setup mode at any one time, and then only for an I/O access to addresses #0100–#0107.

Adaptor setup: (I/O port #96)

7	6	5	4	3	2	1	0
R	0	0	0	S	Slot number		

Bit name	Definition
Slot number	These three bits are binary coded slot number values between 0 and 7.
S	This is the setup enable bit which is high to enable setup mode and low to disable.
R	This is the channel reset bit which asserts the IMS G201 **Reset** signal when high. When high this signal applies reset to all Micro Channel adaptor cards. This bit must be low to communicate the adaptor's POS registers.

POS Register 0: (notSetup and Address0-2 ='000'b)

7	6	5	4	3	2	1	0
1	1	0	1	1	0	IDoption	

This read only register provides the XGA POS identification low byte, returning the value #DB + IDoption.

POS Register 1: (notSetup and Address0-2 ='001'b)

This read only register provides the XGA POS identification high byte. The value returned is #8F.

POS Register 2: (notSetup and Address0-2= '010'b)

7	6	5	4	3	2	1	0
External Memory Addr				IODA			EN

Bit name	Definition
XGA Enable (EN)	When set to 1 identifies that the subsystem is enabled for address decoding for all non POS addresses. When 0, only POS registers can be accessed, all other accesses to the subsystem have no effect.
I/O Device Address (IODA)	This field specifies which set of I/O addresses has been allocated to the IMS G201 registers, i.e. the instance number (refer to Figure 22.7, page 490).
External Memory Address	This field specifies which of sixteen possible 8 Kbytes memory locations has been assigned to the XGA external memory. The external memory occupies the first 7 Kbytes of this 8 Kbytes block, the other 1 Kbyte being occupied by the coprocessor memory-mapped registers (see Figure 22.9, page 491).

POS Register 3: (notSetup and Address0-2= '011'b)

7	6	5	4	3	2	1	0
AV1	Arbitration Level				FE	EM	AV0

Bit name	Definition
EM	External Memory Enable 0 = External Memory Address Decoding Disabled. (See POS Register 2 bits 4-7) 1 = External Memory Address Decoding Enabled. (See POS Register 2 bits 4-7)
FE	Fairness Enable 0 = Micro Channel Fairness Protocol Disabled. 1 = Micro Channel Fairness Protocol Enabled.
Arbitration Level	This 4 bit field is loaded with the 4 bit priority level to be used during Bus Master arbitration.
Avarice	These bits control how the IMS G201 gives up bus ownership of the Micro Channel.

Bits AV1:AV0	Bus release control
00	Release the bus when access is not required
01	Release the bus immediately when preempted if access is not required, otherwise release within 7.8µs.
10	Release the bus within 7.8µs when preempted
11	Reserved

POS Register 4: (notSetup and Address0-2= '100'b)

7	6	5	4	3	2	1	0
Video Memory Base							VE

Bit name	Definition
Video Memory Base Address	This register contains the most significant 7 bits of the address at which the XGA external memory is located. Three more bits are provided by the I/O Device Address in POS byte 1. This gives a Video Memory Base address on a 4Mbyte boundary.
Video Memory Enable (VE)	This bit signifies whether the 4Mbyte aperture is available for use. When this bit is set to 0 the 4Mbyte Aperture is disabled, and when set to 1 the 4Mbyte Aperture is enabled.

POS Register 5: (notSetup and Address0-2 ='101'b)

7	6	5	4	3	2	1	0
1	1	Etiq	SD	1Mbyte Base			

Bit name	Definition
1Mbyte Base	This field specifies where the 1Mbyte Aperture has been positioned in system address space in increments of Mbytes. A 0 in the field will disable the aperture.
SD	When set to 1 this bit will disable Streaming Data transfers on the Micro Channel. When set to 0 Streaming Data transfers are enabled.
Etiquette	When this bit is set to 1 the IMS G201 will obey the Micro Channel rules of Etiquette for bus masters. When this bit is 0 the IMS G201 does not follow the Etiquette rules.

22.9.4 Memory configuration registers

G201 Index	G191 Addr.	Register	Read/ Write
00 01 02	01	Memory configuration 0 Memory configuration 1 Memory configuration 2	Read/ Write

The memory configuration registers (index 00, 01 and 02) should not be used or relied upon in any application software. They are card design specific and are used to configure the chip and will vary depending on the amount and type of VRAM used.

All bits marked '–' are reserved and must be masked out on reads and written to 0 (low) on writes unless otherwise specified.

Memory configuration 0 register (Index: #00)

The memory configuration register 0 sets the video memory port width.

7	6	5	4	3	2	1	0
–	–	–	–	SW	–	PW	

Bit field	Definition
PW (bits 1:0)	Serializer Physical Width. This field determines the width of the VRAM SAM that is actually being used. The encoding is as follows:
SW (bit 3)	Serializer Width. This bit indicates how wide the serializer in the IMS G191 is. A 0 indicates a 32 bit serializer. and a 1 indicates a 64 bit serializer.

Bits 1:0	32 bit Serializer	64 bit Serializer
00	8 bits	16 bits
01	16 bits	32 bits
10	32 bits	64 bits
11	Invalid	Invalid

Memory parameter register (Index: #01)

7	6	5	4	3	2	1	0
–	–	–	–	–	TRF	TRC	TPC

Bit field	Definition
TPC (bit 0)	Page Mode Cycle Time. A 1 extends CAS fall to the next CAS fall from 100ns to 150ns.
TRC (bit 1)	Random Cycle Time. A 1 extends RAS fall to the next RAS fall from 250ns to 300ns. If both TPC and TRC are set to 1 the RAS–RAS time is 350ns).
TRF (bit 2)	Extended Refresh. A 1 extends the time that RAS/CAS are active during a refresh cycle from 100ns to 150ns.

Memory parameter register (Index: #02)

7	6	5	4	3	2	1	0
–	–	–	–	SL	–	–	–

Bit field	Definition
SL (bit 3)	Serializer Length. 0 sets the configuration for a 256 bit serializer. 1 sets the configuration for a 512 bit serializer.

22.10 Hardware interfaces

The IMS G201 display controller interfaces to several other components in an XGA subsystem. These include: the system bus (either an AT bus or a Micro Channel bus); the IMS G191 serializer palette DAC; VRAM; ROM and external registers.

22.10.1 System bus interface

System bus interface for AT bus mode

The system bus interface in AT bus mode, consists of an address bus allowing access to a 16 Mbyte address space, a 16 bit data bus, and control signals to interface directly to AT and ISA bus systems. The IMS G201 supports both slave and master memory cycles on the AT bus. Slave cycles can be 8 or 16 bits depending upon the values written to the POS registers. 16 bit slave memory cycles are always supported when using the 1M aperture, since this aperture must be above the first 1M in the PC's address space. When the coprocessor requires the use of system memory, bus mastership is utilized using one of three 16-bit DMA resources. The IMS G201 as AT bus master controls the bus and supplies addresses for the required 16 bit bus cycles. Figure 22.13 shows the IMS G201 signals used to interface with the AT bus.

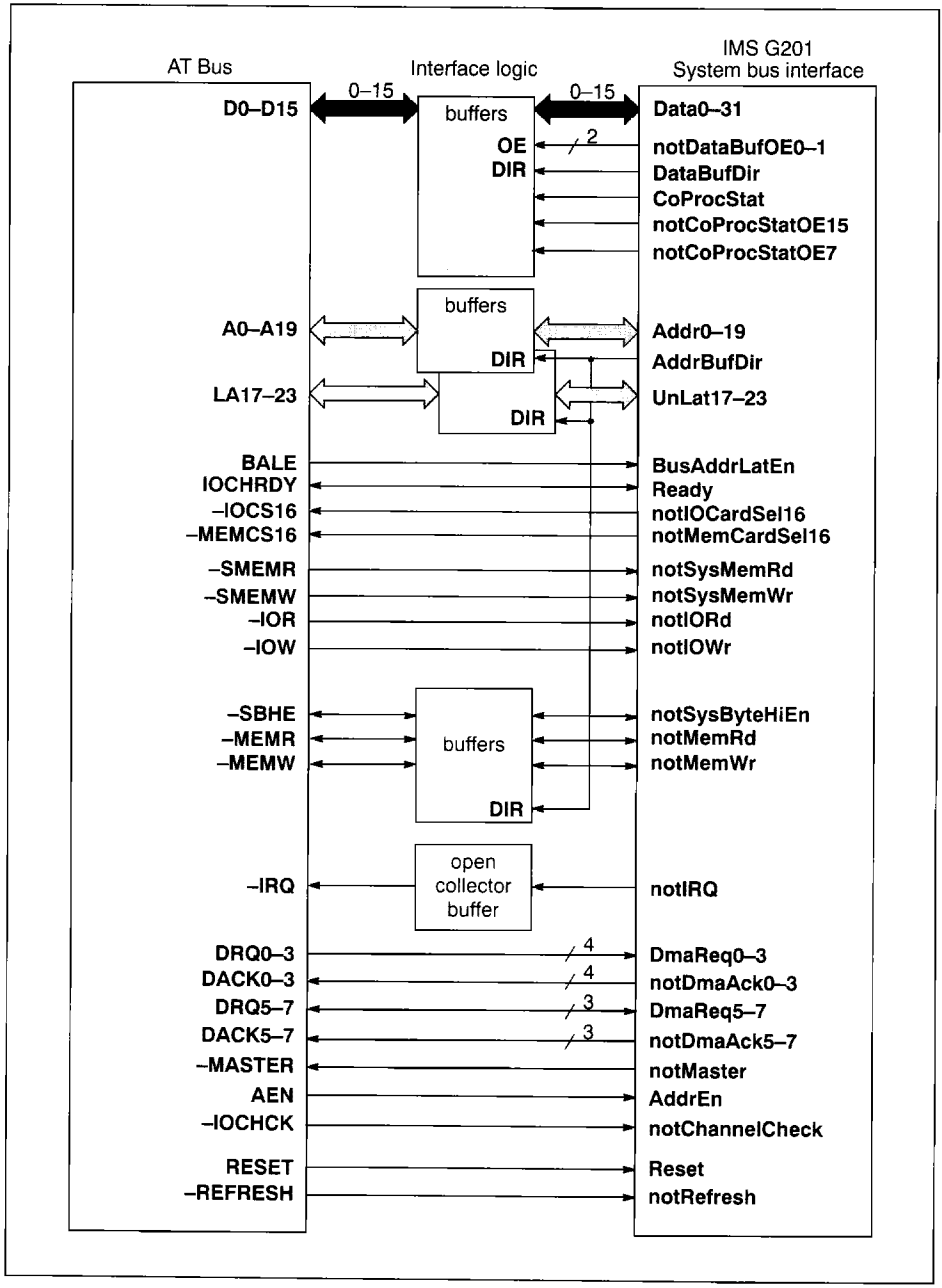

Figure 22.11 IMS G201 system bus interface (AT bus mode)

System bus interface for Micro Channel bus mode

The system bus interface consists of the address, data, and controls defined in the Micro Channel specification. When the coprocessor is being used in system memory, bus mastership is utilized. A bus master controls the bus and supplies addresses for the bus cycles. Either 16 or 32 bit channels are supported. Figure 22.13 shows the IMS G201 signals used to interface with the Micro Channel bus.

The IMS G201 can act either as Master or Slave with either a 16 or 32-bit interface depending on the card configuration. Micro Channel streaming data operation is supported when the IMS G201 is bus master only.

The Micro Channel architecture defines an arbitration procedure through which all prospective bus masters go. The outcome of this arbitration procedure is that one card is granted bus mastership status. This card then controls all cycles on the bus, providing addresses for each cycle or burst of cycles until another card becomes the bus master.

Provision is made within the Micro Channel specification for a slave to extend a cycle when being asked to supply data by using the ready signal.

The IMS G201, in particular, always uses this Channel Ready signal (**CD CHRDY**) in order to force an extended cycle when in slave mode.

Certain signals in the Micro Channel definition must be driven by an open collector device. The arbitration (ARB) signals are an example. The IMS G201 display controller splits these into two signals, an input (**ArbIn**) and an output (**ArbOut**). Figure 22.12 shows how a typical open collector Micro Channel signal would be buffered. The Micro Channel ARB signal is driven by a three-state buffer whose enable is driven by **ArbOut**. Refer to the IBM Micro Channel specification for further details.

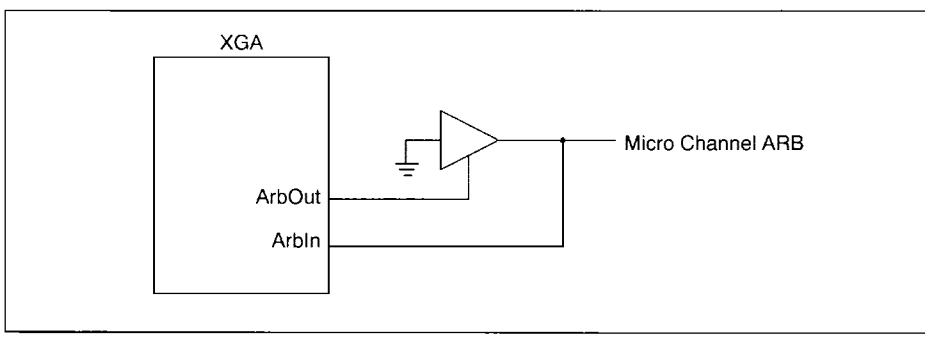

Figure 22.12 External buffer for Micro Channel signals requiring open collector drivers

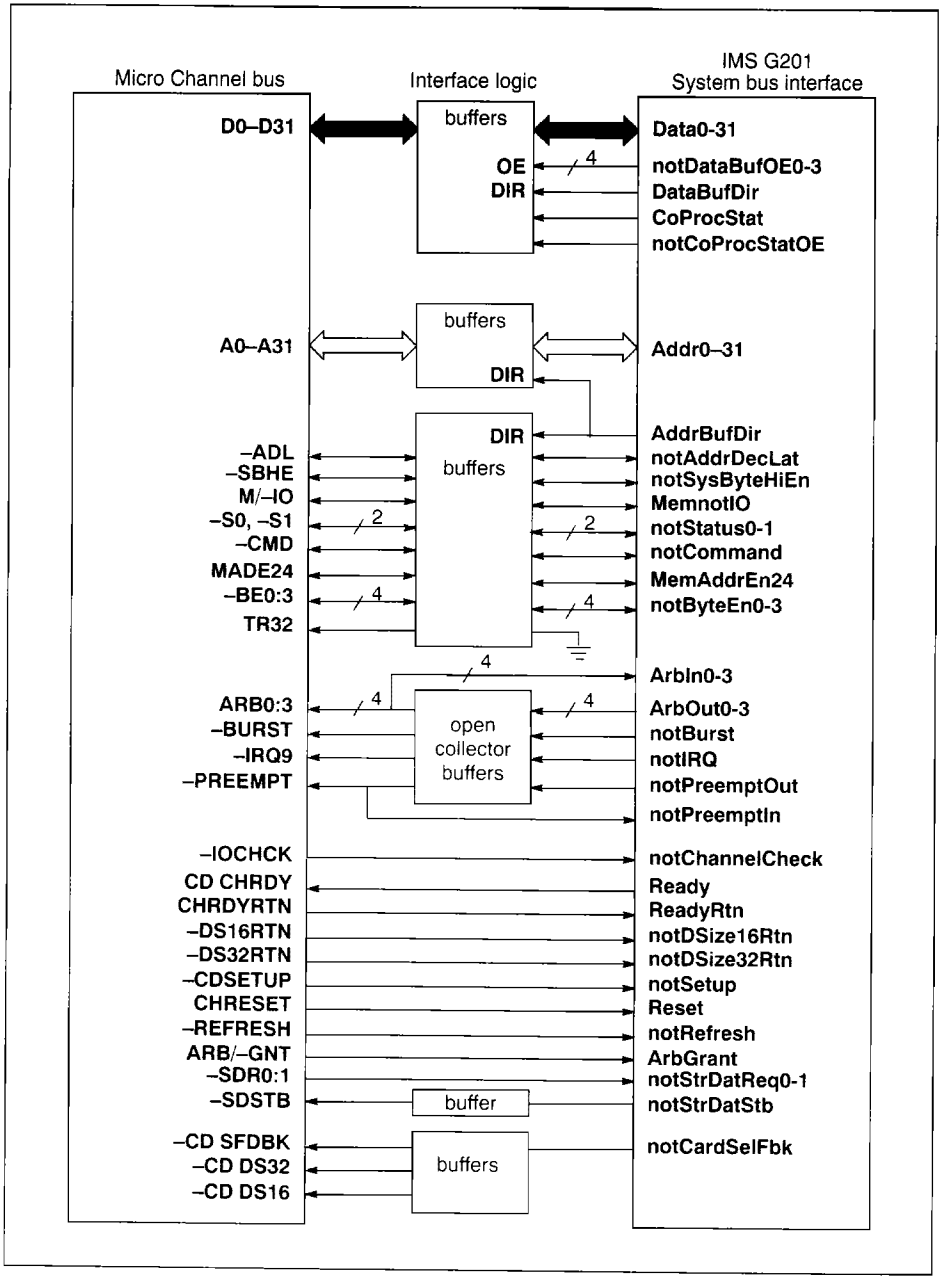

Figure 22.13 IMS G201 system bus interface (Micro Channel bus mode)

22.10.2 VRAM interface

The IMS G201 display controller controls all operations to the VRAM. On the random port, refresh cycles, serializer transfer cycles, system read/write, and coprocessor read/write cycles are performed. On the serial port, the serializer shift clock is provided. The IMS G201 display controller can support VRAM widths of either 16 or 32 bits.

The data bus (**Data0-31**) is shared by the VRAM and the system bus. Isolation buffers are required to allow this dual use. The VRAM data is also used to communicate with the IMS G191 serializer palette DAC, external registers and ROM.

All control signals for the VRAM are generated in the IMS G201 display controller. This includes **notVRAS0-1**, **notVCAS0-1**, **notVOE**, **notVWE0-3** and **VSClk**.

Figure 22.14 shows the connections between the VRAM controller of the IMS G201 and the external VRAM.

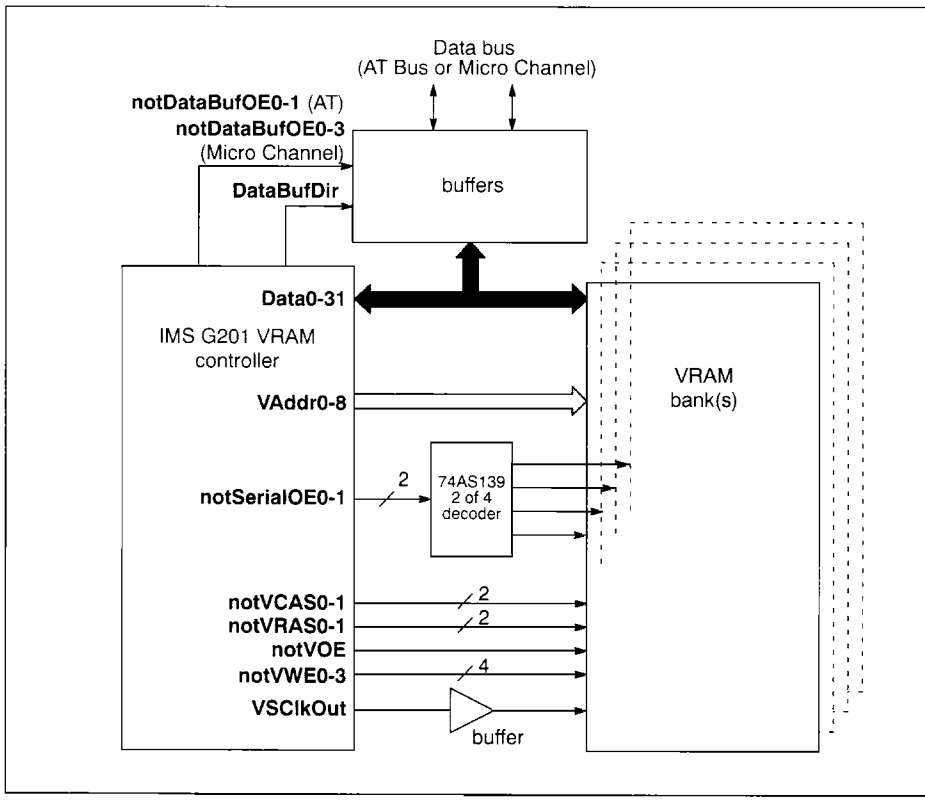

Figure 22.14 IMS G201 VRAM interconnection

VRAM Transfer Cycles

Transfer cycles are generated at the start of every line and every time the VRAM serializer becomes empty. Depending on the screen width and where the VRAM base address was assigned, two transfer cycles are generated at the start of some lines if the serializer becomes empty just after the start of a line.

Support for multiple VRAM banks

The IMS G201 now supports up to 4 Mbytes of VRAM consisting of devices using nine row and nine column address lines. The VRAM internal architecture must consist of a number of 512 x 512 (256 Kbytes) memory arrays, typically 256K x 4, since the IMS G201 supports a 9-bit multiplexed VRAM address bus. Care should be taken not to exceed the IMS G201 pin output loading characteristics, given in Section 22.13.3, when connecting multiple VRAM devices.

The IMS G201 framestore manager supports up to four banks of VRAM populating the full 32-bit data and pixel path using **notVRAS0**, **notVRAS1**, **notVCAS0** and **notVCAS1** (pins formerly assigned as **notVRAS**, **N/C**, **notVCAS** and **N/C**). The four VRAM banks are configured using these strobes as follows:

Bank 0	Bank 1	Bank 2	Bank 3
notVRAS0	notVRAS0	notVRAS1	notVRAS1
notVCAS0	notVCAS1	notVCAS0	notVCAS1

The VRAM column and row address strobes are coded as shown in Table 22.9. The column address coding allows any bank in the XGA subsystem to be uniquely accessed (**notVCAS0-1** - H, **notVRAS0-1** - H) whilst the second row addressed bank (**notVCAS0-1** - L, **notVRAS0-1** - H) is refreshed at the row address presented.

VRAM bank	notVRAS0	notVRAS1	notVCAS0	notVCAS1
0	L	H	L	H
1	L	H	H	L
2	H	L	L	H
3	H	L	H	L

Table 22.9 Coding of VRAM column and row address strobes

In addition to supporting multiple banks on the random access port the IMS G201 provides coded serial output enable strobes (**notSerialOE0-1**) to multiplex pixel data from any one of four VRAM serial ports. Typically, an external decoder with inverting outputs ($^1/_2$ of 74AC139) is used to perform the serial output enable function of the required VRAM banks as defined in Table 22.10.

notSerialOE0	notSerialOE1	Bank selected
0	0	0
0	1	1
1	1	2
1	0	3

Table 22.10 Coding of VRAM serial output enable strobes

22.10.3 IMS G191 serializer palette DAC interface.

Figure 22.15 shows the signals used within the IMS G201 to connect the IMS G191 serializer palette DAC.

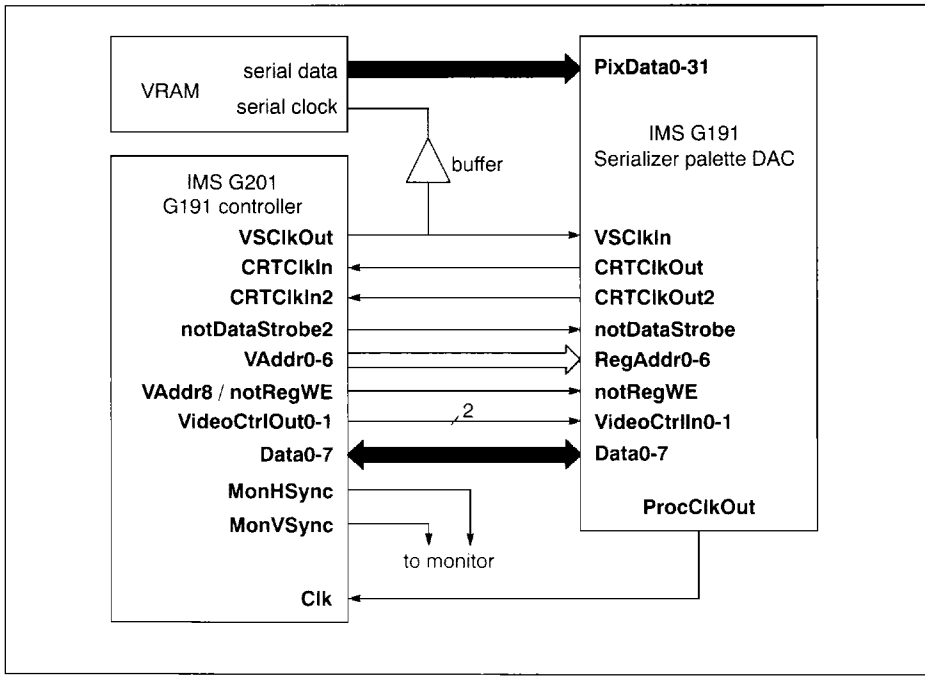

Figure 22.15 IMS G201 interface to the IMS G191

The **notDataStrobe2** output from the IMS G201 is dedicated to the IMS G191. It is used to strobe addresses and control code data (carried on the **VAddr0-6** bus) from the IMS G201 to the IMS G191. It is used to communicate register contents programmed by the host processor and decoded in the IMS G201. A low sent on this pin to the IMS G191 indicates that the IMS G191 should perform the action defined by the **VAddr0-6** and **notRegWE** pins.

The **notRegWE** pin is driven by bit 8 (**VAddr8**) of the VRAM address bus during accesses between the IMS G201 and IMS G191. It determines whether a read or write cycle is being executed. When low, indicating a write to the IMS G191, it inputs the data (**Data0-7**) into the IMS G191 addressed parameter register. When high, indicating a read from the IMS G191, it outputs the contents of the addressed parameter register onto the data bus.

The data bus (**Data0-7**) is bi-directional between the IMS G201 and the IMS G191 and transfers parameter register data.

G201 writes to G191 registers

For IMS G191 register writes, data is passed from the IMS G201 to the IMS G191 in byte-wide chunks over the data bus (**Data0-7**). All 8 bits of data are passed to the IMS G191 for shared registers, as well as for the other registers. For shared registers the IMS G201 also latches its required data at the same time.

Bus (AT bus or Micro Channel) registers in the IMS G201 and the IMS G191 which have duplicate bits are written to in both chips. The slowest write controls the **Ready** signal to the system bus. G201 writes to G191 registers are shown in Figure 22.16.

Write to G191 register strobes

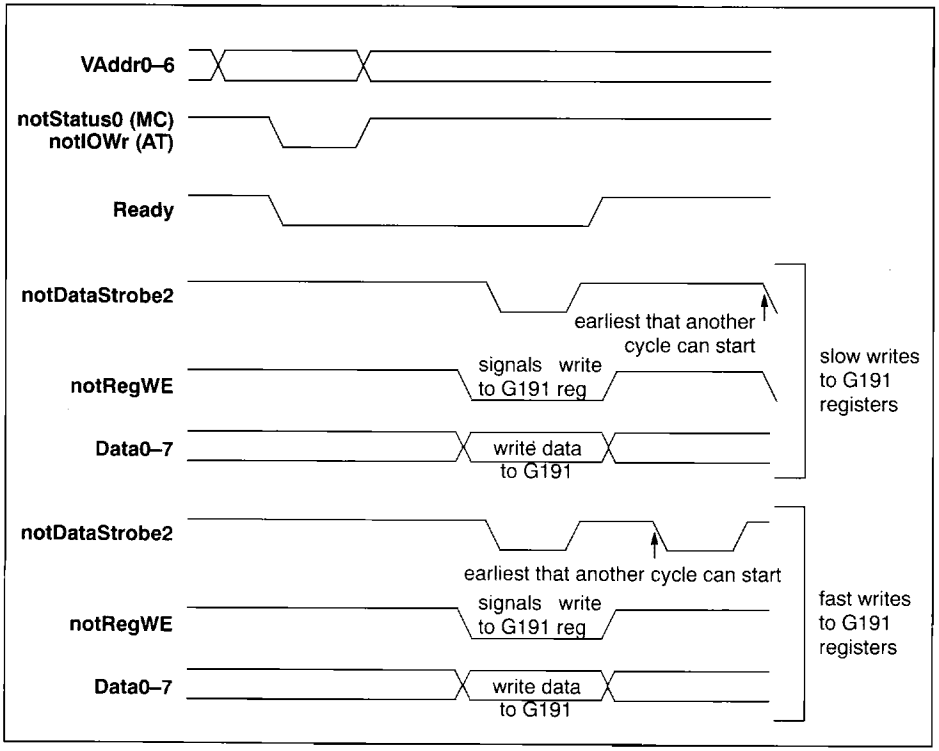

Figure 22.16 G201 writes to G191 registers

G201 reads of G191 registers

For IMS G191 register reads data is read from the IMS G191 via the data bus and latched in the IMS G201. Any shared registers are then OR'ed to ensure data consistency. Any bits which are duplicated between registers in the IMS G201 and IMS G191 are also OR'ed. The IMS G201 then performs any necessary operations on the data before passing it to the system bus. G201 reads of G191 registers are shown in Figure 22.17.

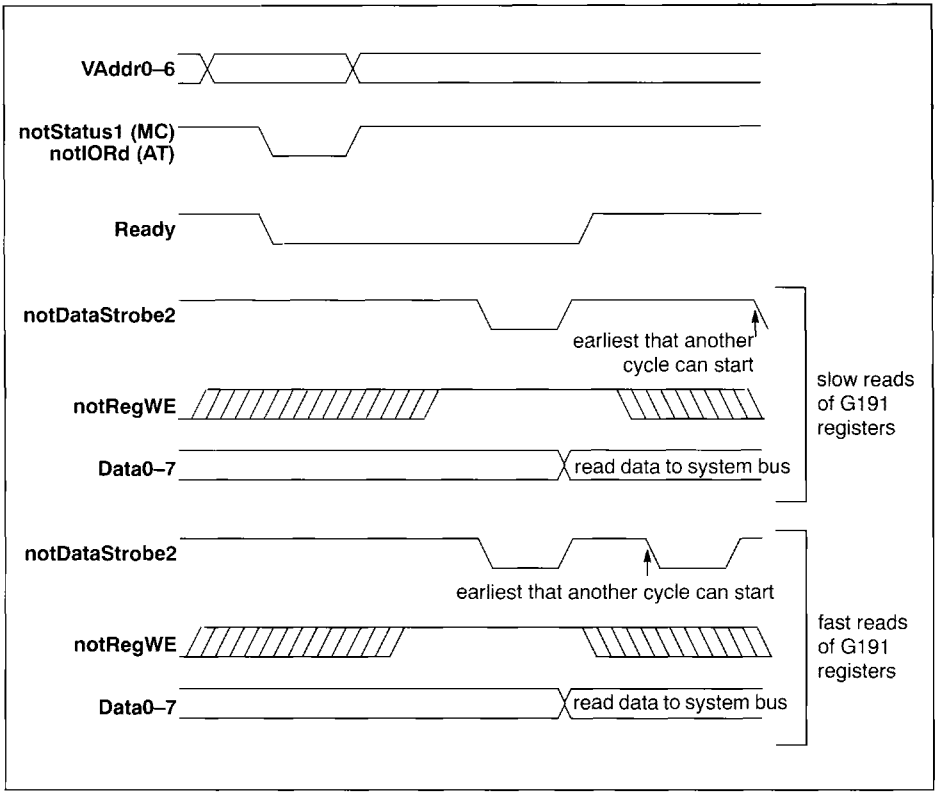

Figure 22.17 G201 reads of G191 registers

22.10.4 External memory and register interface

Reads and writes to external registers and static memory are handled in a similar way to IMS G191 register reads and writes. The **notDataStrobe1** signal strobes low to cause reads and writes to/from external memory (typically PROM) and external registers. This signal is qualified by one of the data bits (**Data28-31**) to select a particular type of operation, as follows:

Data28	External memory write
Data29	External memory read
Data30	External register write
Data31	External register read

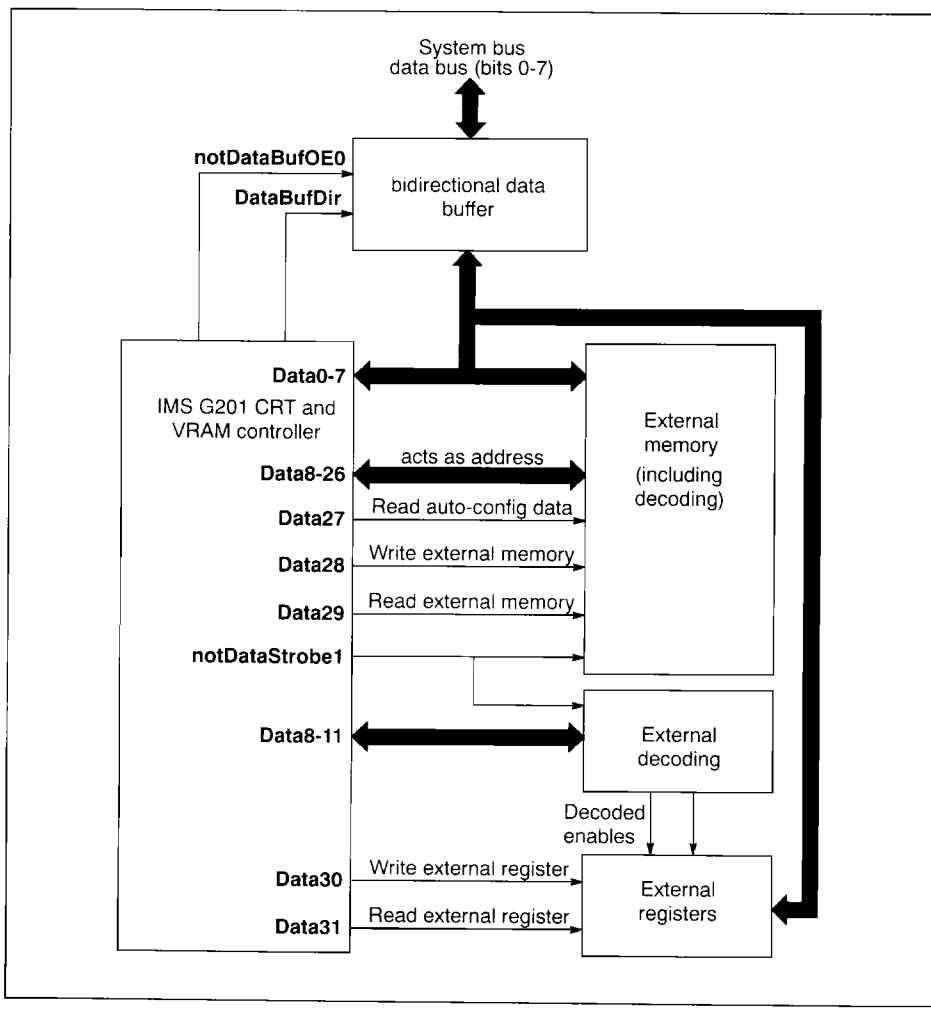

Figure 22.18 IMS G201 external memory and register interface

External memory accesses

The IMS G201 supports an external ROM or RAM device and can map it into system address space. For a Micro Channel bus system an 8K space within the 128K ROM area (C0000–DFFFF) provides a ROM decode. For an AT bus system the ROM decode is widened to 32K.

When the external storage is accessed, the IMS G201 generates a low pulse on **notDataStrobe1**. During a read from external storage, **notDataStrobe1** will be qualified by **Data29** being low. A write will be qualified by **Data28** being low.

This is the mechanism for supporting an adapter BIOS ROM. Programmable Option Select (POS) registers define the decoding range of the external storage.

The address for the external storage access is driven on **Data8-20** and data is driven on **Data0-7**.

External register accesses

Some implementations of the XGA subsystem require the use of external registers accessible by the system processor. The IMS G201 assists in this by providing a range of decodes for which a strobe signal and qualifiers are generated. External register operation is similar to external memory access. **notDataStrobe1** is the strobe pulse that is qualified by **Data30** for writes and **Data31** for reads. **Data8-11** are available for decoding specific registers, as defined below.

XGA indexed register 21xA	Data8-11 external register address	Description
70	0	External clock select register
71	1	ROM paging
72-7F	2-F respectively	External registers

22.11 Timing reference guide for AT bus mode

22.11.1 AT bus timings

The following timing diagrams and tables show AT bus timings at the channel connector. IMS G201 signal names are shown in the left-hand and AT bus names in the right-hand column.

Slave bus cycles

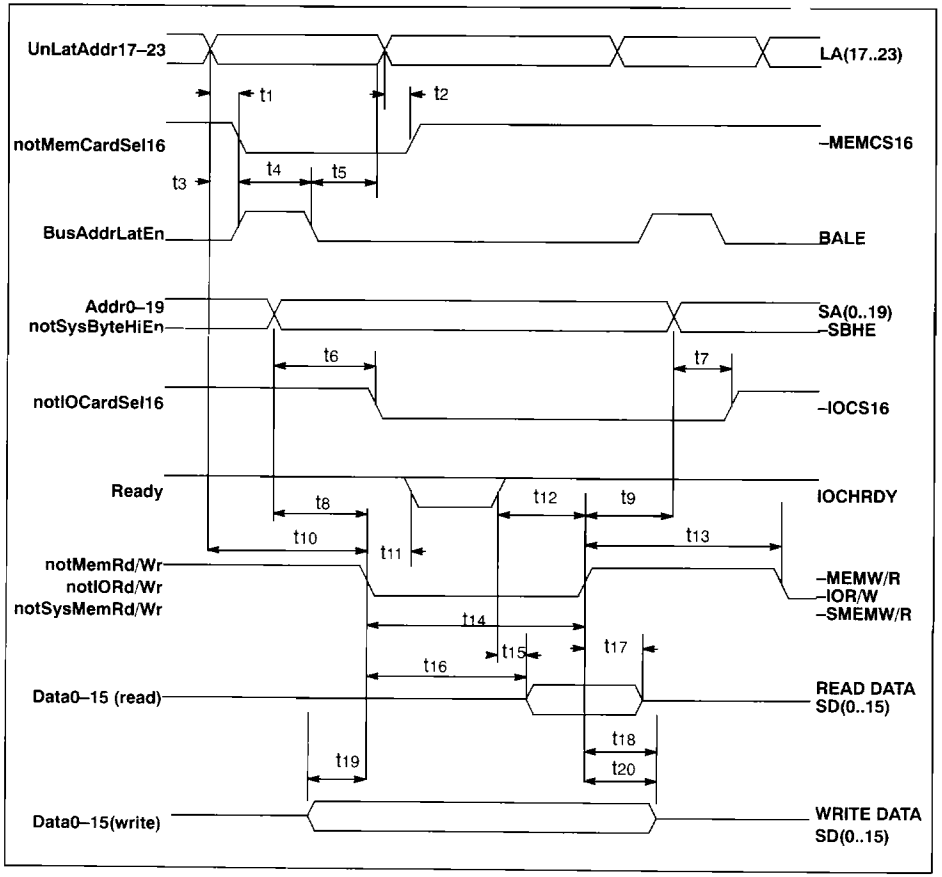

Figure 22.19 Slave bus cycle waveforms

Symbol	Parameter	Min	Max	Units
t1	**notMemCardSel16** active from **UnLatAddr17–23**		43†	ns
t2	**notMemCardSel16** hold from **UnLatAddr17–23**	0		ns
t3	**UnLatAddr17–23** setup to **BusAddrLatEn**	50		ns
t4	**BusAddrLatEn** pulse width	50		ns
t5	**UnLatAddr17–23** hold after **BusAddrLatEn**	15		ns
t6	**notIOCardSel16** active from **Addr0–15**		48†	ns
t7	**notIOCardSel16** hold from **Addr0–15**	0		ns
t8 a	**Addr1–19** setup to memory command strobe active **Addr1–19** setup to I/O command strobe active	28 28		ns
t8 b	**notSysByteHiEn, Addr0** setup to memory command strobe active **notSysByteHiEn, Addr0** setup to I/O command strobe active	28 28		ns
t9	**Addr0–19** and **notSysByteHiEn** hold after command strobe inactive	20		ns
t10	**UnLatAddr17–23** setup to command strobe active	109		ns
t11	**Ready** inactive from command strobe active (Mem) **Ready** inactive from command strobe active (I/O)		35 35	ns
t12	Command strobe inactive from **Ready** active	125		ns
t13	Command separation	97		ns
t14	Memory write command pulse width (**Ready** active) I/O write command pulse width (**Ready** active) Memory read command pulse width (**Ready** active) I/O read command pulse width (**Ready** active)	165 115 165 115		ns
t15	Read data active from **Ready** active		64	ns
t16	Memory read data access (**Ready** active) I/O read data access (**Ready** active)		122 72	ns
t17	Read data hold after command inactive	0		ns
t18	Data bus off after read command strobe inactive		30	ns
t19	Memory write data setup to command strobe active I/O write data setup to command strobe active	–56 –56		ns
t20	Write data hold after command strobe inactive	15		ns

†These timings assume a maximum load of 90 pF.

Table 22.11 Slave bus cycle timing values

Master bus cycle waveforms

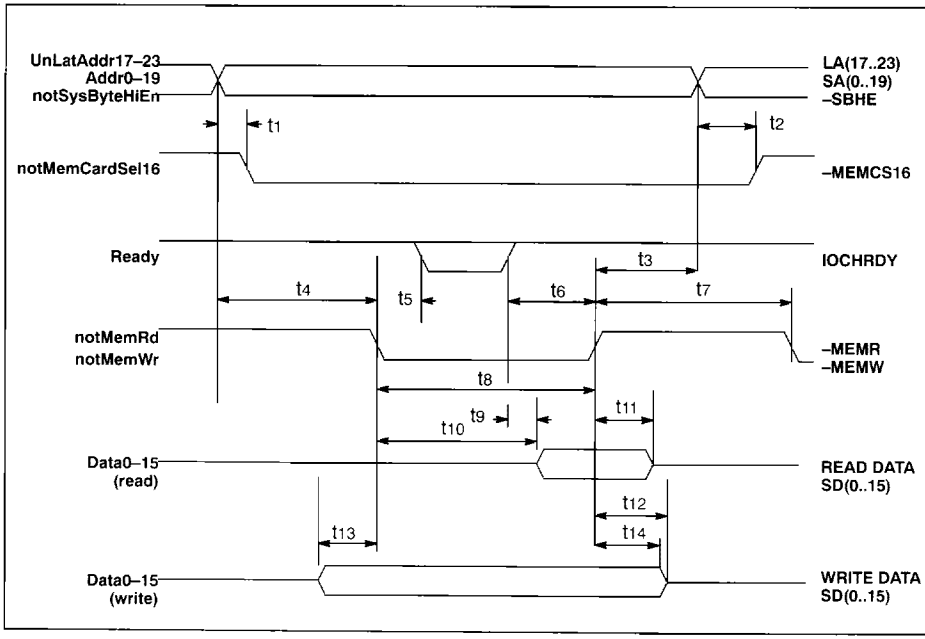

Figure 22.20 Master bus cycle waveforms

Symbol	Parameter	Min	Max	Units
t1	**notMemCardSel16** valid from address		80	ns
t2	**notMemCardSel16** hold from address	0		ns
t3	Address hold after command	42		ns
t4	Address setup to command	91		ns
t5	**Ready** inactive from command		59	ns
t6	Command strobe inactive from **Ready** active	125		ns
t7	Command separation	159		ns
t8	Write Command pulse width Read Command pulse width	219 219		ns
t9	Read data valid from **Ready** active	85		ns
t10	Read data access		195	ns
t11	Data bus off after read command strobe inactive		30	ns
t12	Data bus off after write command strobe inactive		75	ns
t13	Write data setup to command	0		ns
t14	Write data hold after command	25		ns

Table 22.12 Master bus cycle timing values

Bus Arbitration

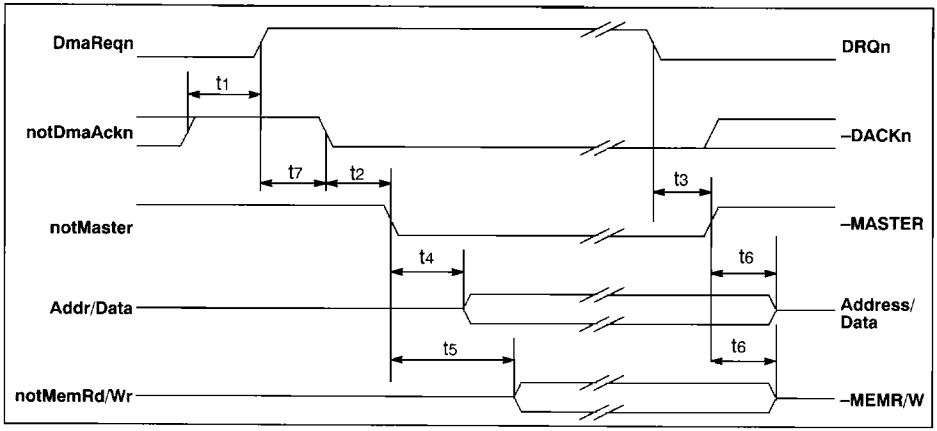

Figure 22.21 Bus arbitration waveforms

Symbol	Parameter	Min	Max	Units
t1	**DmaReqn** active from **notDmaAckn** inactive	0		ns
t2	**notMaster** active from **notDmaAckn** active	0		ns
t3	**notMaster** inactive from **DmaReqn** inactive		100	ns
t4	Address/data driven from **notMaster** active	note 1		ns
t5	Command signals driven from **notMaster** active	note 2		ns
t6	Bus signals tri–stated from **notMaster** inactive		0	ns
t7	**notDmaAckn** active from **DmaReqn**	note 3		ns

Table 22.13 Bus arbitration timing values

Notes

1 Address and data signals must not be driven before 1 system bus clock cycle after **notMaster** is asserted. (125ns on an 8MHz AT).

2 Control signals must not be driven before 2 system bus clocks after **notMaster** is asserted. (250ns on an 8MHz AT).

3 The delay from bus request to grant depends on the system design, but is typically 1.7 microseconds minimum for a 16 bit DMA channel on an 8MHz AT.

22.12 Timing reference guide for Micro Channel bus mode

22.12.1 System bus interface timings

This section provides timing diagrams for the basic I/O and memory cycles. For Figures 22.22 and 22.23 IMS G201 signal names are shown in the left-hand and Micro Channel names in the right-hand column.

I/O and memory cycle timings for IMS G201 as Micro Channel bus master

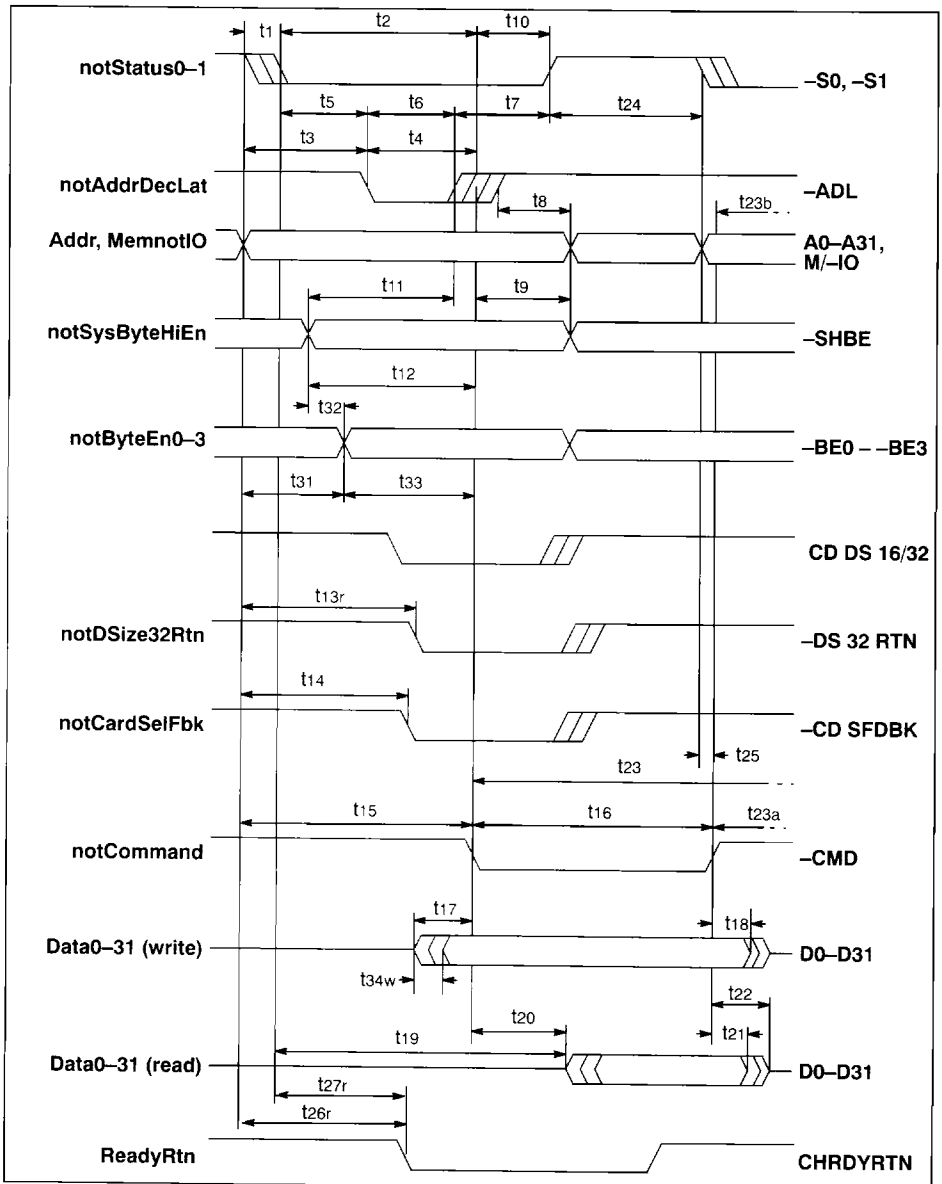

Figure 22.22 I/O and memory cycle timings for IMS G201 as bus master

Symbol	Parameter	Micro Channel		IMS G201		Units
		Min	Max	Min	Max	
t1	**notStatus0-1** active from **Addr, MemnotIO** valid	10		20		ns
t2	**notCommand** active from **notStatus0-1** active	55		65		ns
t3	**notAddrDecLat** active from **Addr, MemnotIO** valid	45		55		ns
t4	**notAddrDecLat** active to **notCommand**	40		50		ns
t5	**notAddrDecLat** active from **notStatus0-1** active	12		22		ns
t6	**notAddrDecLat** pulse width	40		45		ns
t7	**notStatus0-1** hold from **notAddrDecLat** inactive	25		35		ns
t8	**Addr, MemnotIO** hold from **notAddrDecLat inactive**	25		31		ns
t9	**Addr, MemnotIO** hold from **notCommand** active	30		36		ns
t10	**notStatus0-1** hold from **notCommand** active	30		40		ns
t11	**notSysByteHiEn** setup to **notAddrDecLat** inactive	40		50		ns
t12	**notSysByteHiEn** setup to **notCommand** active	40		50		ns
t13r	**notDSize32Rtn** valid from **Addr, MemnotIO** valid		75		88	ns
t14	**notCardSelFbk** valid from **Addr, MemnotIO** valid				*	
t15	**notCommand** active from **Addr** valid	85		95		ns
t16	**notCommand** pulse width	90		95		ns
t17	Write **Data0-31** setup to **notCommand** active	0		10		ns
t18	Write **Data0-31** hold from **notCommand** inactive	30		40		ns
t19	**notStatus0-1** to Read **Data0-31** valid		125		138	ns
t20	Read **Data0-31** from **notCommand** active		60		73	ns
t21	Read **Data0-31** hold from **notCommand** inactive	0		−10		ns
t22	Read data bus tri-state from **notCommand** inactive		40		50	ns
t23	**notCommand** active to next **notCommand** active	190		195		ns
t23a	**notCommand** inactive to next **notCommand** active	80		90		ns
t23b	**notCommand** inactive to next **notAddrDecLat** active	40		50		ns
t24	Next **notStatus0-1** active from **notStatus0-1** inactive	30		40		ns
t25	Next **notStatus0-1** active to **notCommand** inactive		20		10	ns
t26r	**ReadyRtn** inactive from **Addr. MemnotIO** valid		80		90	ns
t27r	**ReadyRtn** inactive from **notStatus0-1** valid and previous **notCommand** inactive	0	50	−10	60	ns
t31	**notByteEn0-3** active from **Addr**		40		30	ns
t32	**notByteEn0-3** active from **notSysByteHiEn**, A0, A1 active		30		20	ns
t33	**notByteEn0-3** active to **notCommand** active	10		20		ns
t34w	Write **Data0-31** setup to write **Data0-31** hold	0	15		*	

*This is a Micro Channel system timing, for details refer to the Micro Channel specification

Table 22.14 I/O and memory cycle timings for IMS G201 as bus master

I/O and memory cycle timings for IMS G201 as Micro Channel bus slave

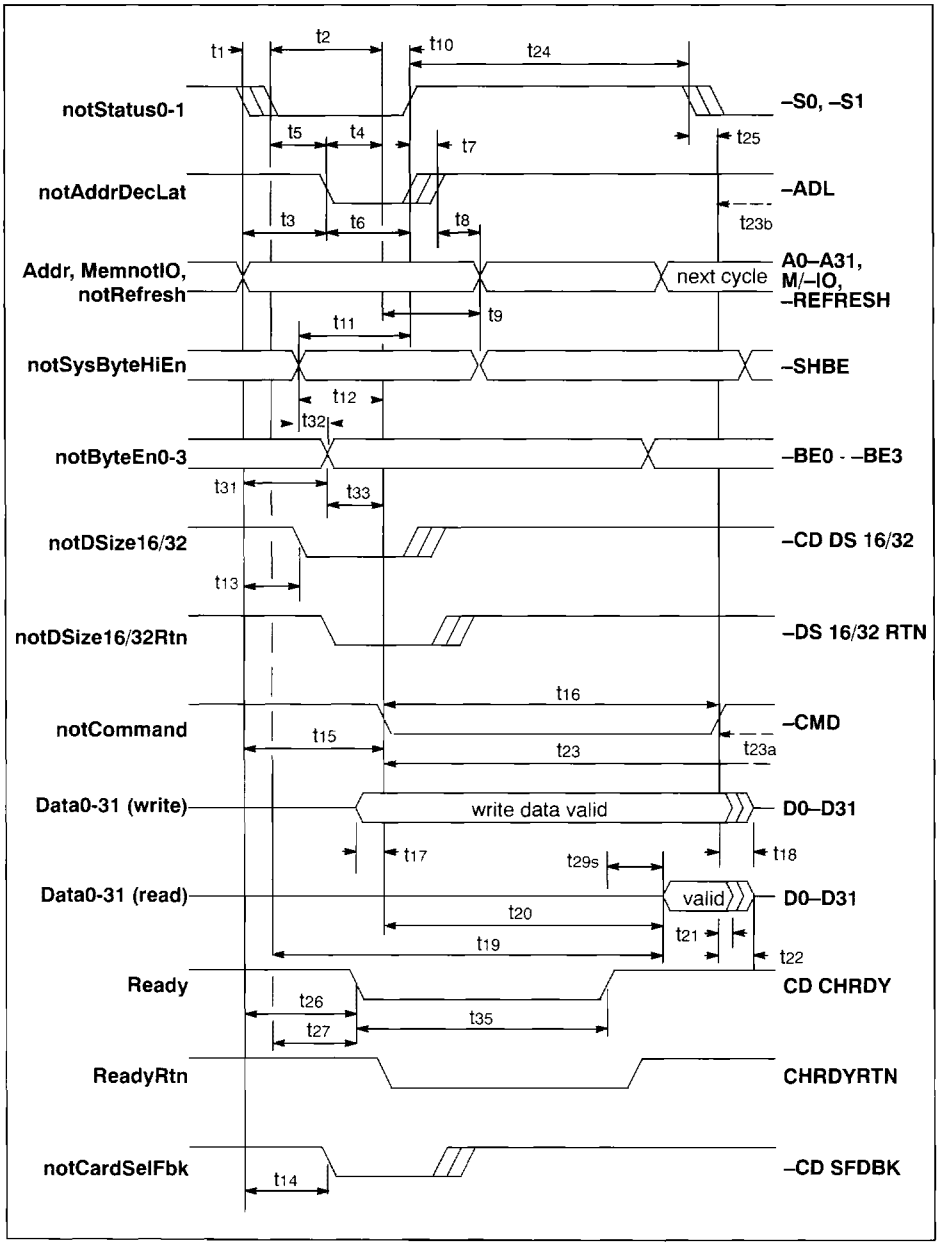

Figure 22.23 I/O and memory cycle for IMS G201 as bus slave

Symbol	Parameter	Micro Channel		IMS G201		Units	Notes
		Min	Max	Min	Max		
t1	**notStatus0-1** active from **Addr,MemnotIO, notRefresh** valid	10		0		ns	
t2	**notCommand** active from **notStatus0-1** active	55		45		ns	
t3	**notAddrDecLat** active from **Addr, MemnotIO, notRefresh** valid	45		35		ns	
t4	**notAddrDecLat** active to **notCommand**	40		30		ns	
t5	**notAddrDecLat** active from **notStatus0-1** active	12		2		ns	
t6	**notAddrDecLat** pulse width	40		30		ns	
t7	**notStatus0-1** hold from **notAddrDecLat** inactive	25		15		ns	1
t8	**Addr,MemnotIO, notRefresh, notSysByteHiEn** hold from **notAddrDecLat** inactive	25		15		ns	
t9	**Addr,MemnotIO, notRefresh, notSysByteHiEn** hold from **notCommand** active	30		20		ns	
t10	**notStatus0-1** hold from **notCommand** active	30		20		ns	1
t11	**notSysByteHiEn** setup to **notAddrDecLat** inactive	40		30		ns	
t12	**notSysByteHiEn** to **notCommand** active	40		30		ns	
t13	**notDsize16/32** valid from **Addr,MemnotIO** valid		55		42	ns	
t14	**notCardSelFbk** valid from **Addr,MemnotIO** valid		60		42	ns	
t15	**notCommand** active from **Addr** valid	85		75		ns	
t16	**notCommand** pulse width	190				ns	2
t17	Write **Data0-31** setup to **notCommand** active	0		−10		ns	
t18	Write **Data0-31** hold from **notCommand** inactive	30		20		ns	
t19	**notStatus0-1** to Read **Data0-31** valid		125		115	ns	
t20	Read **Data0-31** valid from **notCommand** active		60			ns	
t21	Read **Data0-31** hold from **notCommand** inactive	0		10		ns	
t22	Read **Data0-31** bus tri-state from **notCommand** inactive		40		30	ns	
t23	**notCommand** active to next **notCommand** active	190				ns	
t23a	**notCommand** inactive to next **notCommand** active	80		70		ns	
t23b	**notCommand** inactive to next **notAddrDecLat** active	40		30		ns	
t24	Next **notStatus0-1** active from **notStatus0-1** inactive	30		20		ns	
t25	Next **notStatus0-1** active to **notCommand** inactive		20		30	ns	
t26	**CD CHRDY** valid from **Addr** valid		60		53	ns	
t27	**CD CHRDY** valid from **notStatus0-1** valid		30		23	ns	
t29s	Read **Data0-31** valid from **Ready**		60		50	ns	
t31	**notByteEn0-3** active from **Addr** valid (32bit masters only)		40		50	ns	
t32	**notByteEn0-3** active from **notSysByteHiEn, A0, A1** active		30		40	ns	
t33	**notByteEn0-3** active to **notCommand** active	10		0		ns	
t35	**CD CHRDY** valid from **-CD CHRDY**		3.5		3.5	µs	

Notes:

1 A bus master must deactivate **–S0,1** as soon as possible after the hold time specified by t7 and t10, and prior to the deactivation of **–CMD**. This deactivation must be independent of **CHRDYRTN**.

2 All slave cycles are extended except for accesses to the external polling register. These are default cycles (**–CMD** pulse width is 90ns min).

Table 22.15 I/O and memory cycle for IMS G201 as bus slave

IMS G201 Micro Channel buffer timings in slave mode

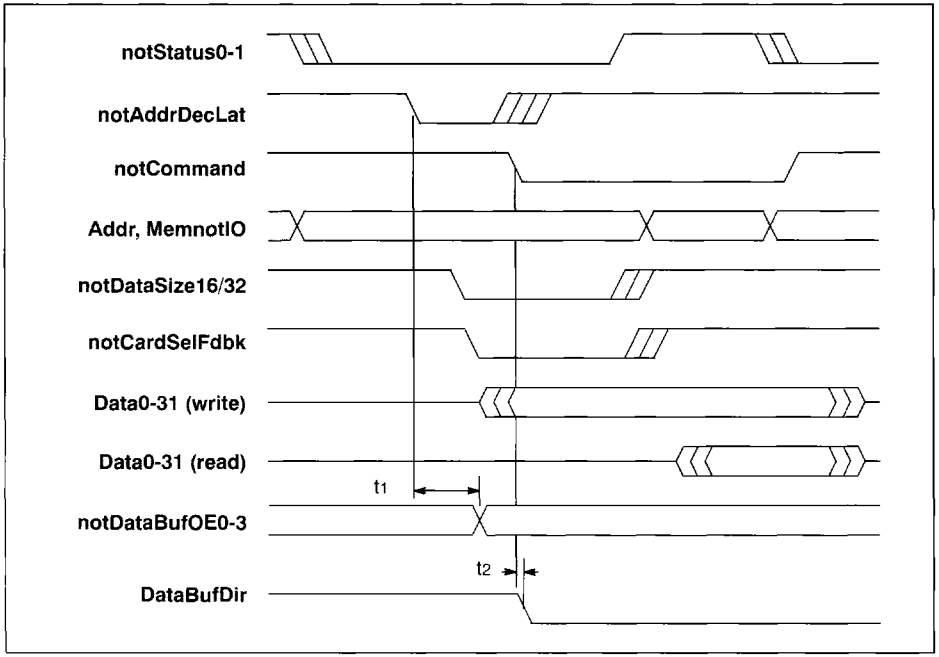

Figure 22.24 IMS G201 Micro Channel buffer timings in slave mode

Symbol	Parameter	Min	Max	Unit	Notes
t_1	**AddrDecLat** to **notDataBufOE0-3** change	7	29	ns	
t_2	**Command** to **DataBufDir** change	5	18	ns	

Table 22.16 IMS G201 Micro Channel buffer timings in slave mode

Timings for Micro Channel arbitration cycle

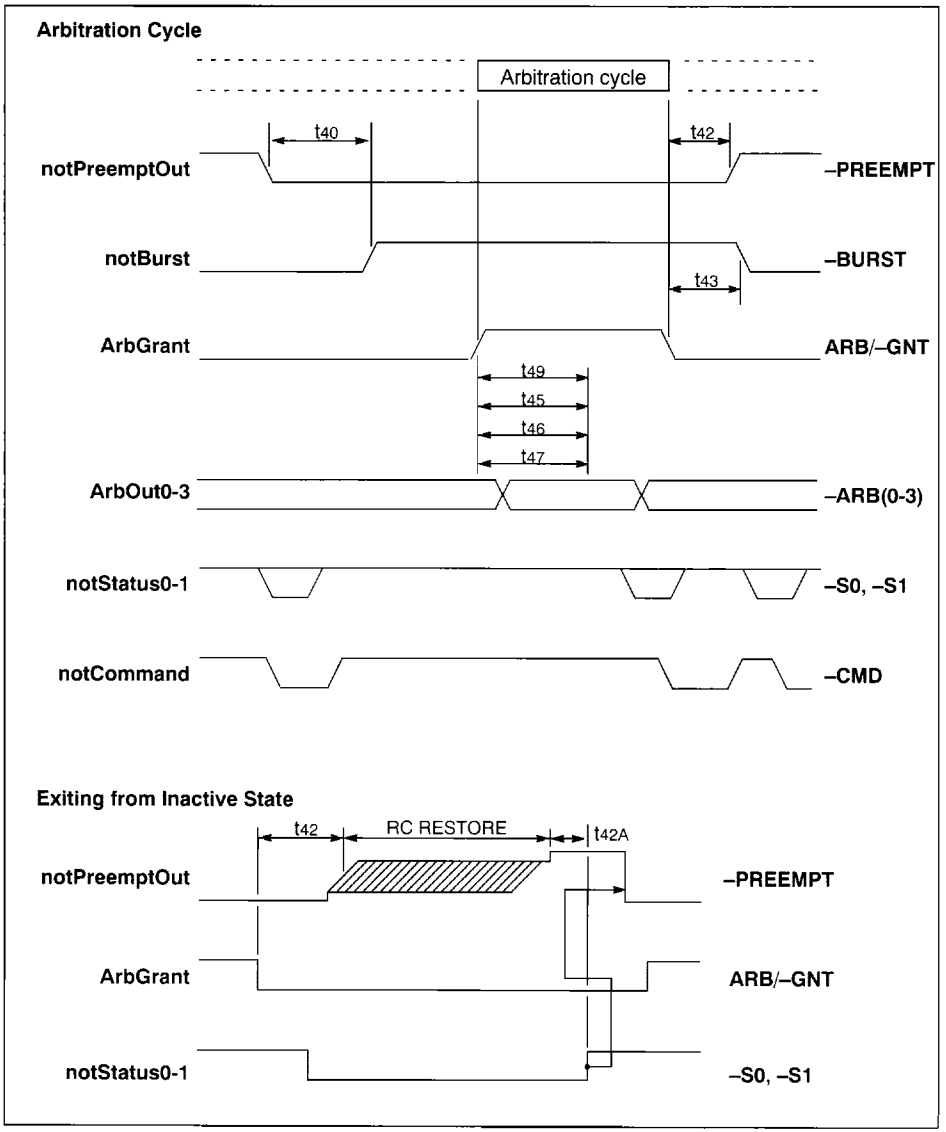

Figure 22.25 Arbitration cycle

Symbol	Parameter	Micro Channel		IMS G201		Units	Notes
		Min	Max	Min	Max		
t_{40}	**notPreempt** active (low) to end of transfer	0	7.8	0	7.5	µs	
t_{42}	**notPreempt** inactive (high) from **ArbGrant** low	0	50	0	40	ns	
t_{42A}	**notPreempt** inactive (high) to Status inactive	20		30		ns	1
t_{43}	**notBurst** active (low) from **ArbGrant** low (by bursting DMA slave)		50		40	ns	
t_{45}	Driver turn-on delay from **ArbGrant** high	0	50	0	40	ns	
t_{45A}	Driver turn-on delay from lower priority line	0	50	0	40	ns	
t_{46}	Driver turn-off delay from **ArbGrant** high	0	50	0	40	ns	
t_{47}	Driver turn-off delay from lower priority line	0	50	0	40	ns	
t_{49}	Tri-state drivers from **ArbGrant** high		50		40	ns	

Note:

1 t_{42A} represents the timing requirement after the resistor-capacitor line delay. This window is available for devices to detect inactive **–PREEMPT** and exit from the inactive state after the rising edge of **–S0, S1**.

Table 22.17 Arbitration cycle timings

Timings for Micro Channel streaming data mode

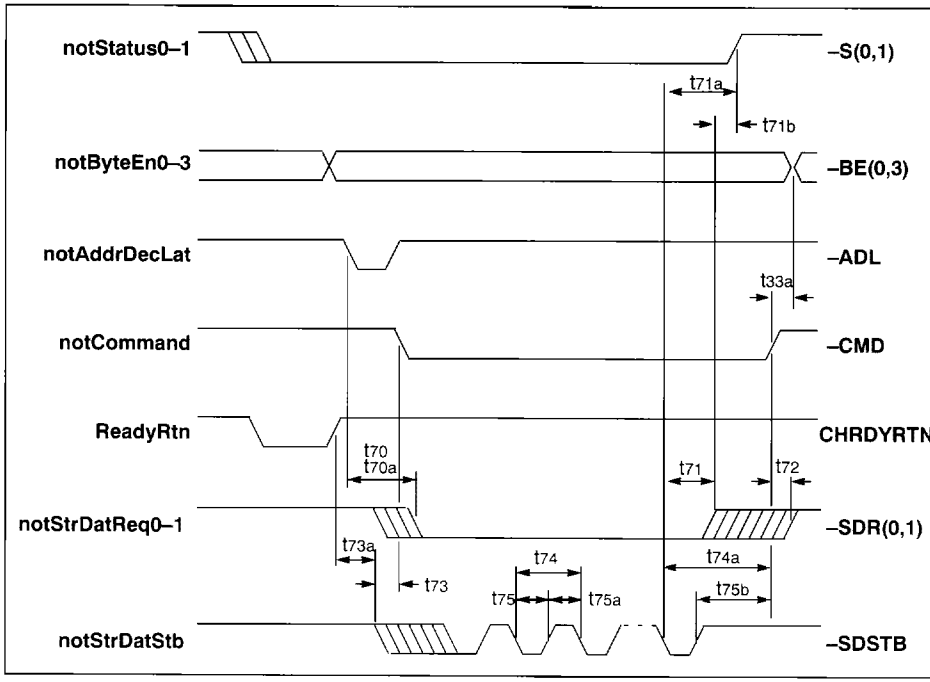

Figure 22.26 Streaming mode timing diagram for streaming data cycle basic signal sequence

Symbol	Parameter	Micro Channel		IMS G201		Units
		Min	Max	Min	Max	
t33a	**notByteEn0-3** hold from **notCommand** inactive	10		20		ns
t70	**notStrDatReq0–1** valid from **notAddrDecLat** active (slave)	0	40	–10	50	ns
t70a	**notStrDatReq0–1** valid from **notAddrDecLat** active (master)	0	115	–10	125	ns
t71	**notStrDatReq0–1** inactive from last **notStrDatStb** fall	0	40	–10	50	ns
t71a	**notStatus0-1** inactive from last **notStrDatStb** fall		10		10	ns
t71b	**notStrDatReq0–1** inactive from **notStatus0-1** inactive	0	40	–10	50	ns
t72	**notStrDatReq0–1** tristate from **notCommand** inactive	0	40	–10	50	ns
t73	**notStrDatStb** active to **notCommand** active		10		0	ns
t73a	**notStrDatStb** active from **ReadyRtn** active	0		10		ns
t74	**notStrDatStb** period	100		100		ns
t74a	**notCommand** inactive from last **notStrDatStb** fall	100		110		ns
t75	**notStrDatStb** active	35		40		ns
t75a	**notStrDatStb** inactive	35		40		ns
t75b	**notStrDatStb** inactive to **notCommand** inactive	35		45		ns

Table 22.18 Streaming mode timings for streaming data cycle basic signal sequence

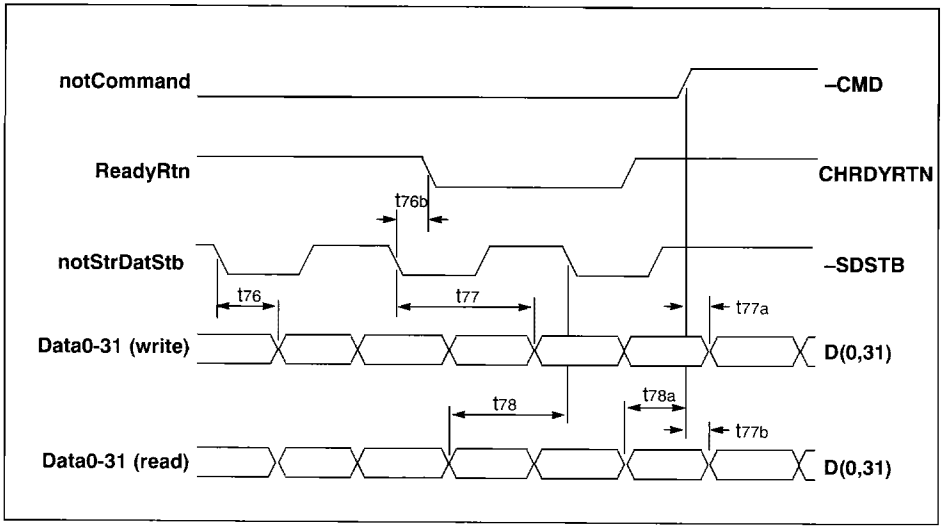

Figure 22.27 Streaming mode timing diagram for streaming data clocking

Symbol	Parameter	Micro Channel		IMS G201		Units
		Min	Max	Min	Max	
t76	**Data0-31** (send) valid from **notStrDatStb** fall		60		50	ns
t76b	**ReadyRtn** valid from **notStrDatStb** fall	3	45	–2	50	ns
t77	**Data0-31** (send) hold from **notStrDatStb** fall	10		20		ns
t77a	**Data0-31** (write) hold from **notCommand** inactive	11		21		ns
t77b	**Data0-31** (read) hold from **notCommand** inactive	7		0		ns
t78	**Data0-31** (receive) valid before **notStrDatStb** fall	25		20		ns
t78a	**Data0-31** (receive) valid before **notCommand** inactive	25		20		ns

Table 22.19 Streaming mode timings for streaming data clocking

22.12.2 VRAM interface timings

VRAM Read/Write Timings

All accesses to the random read/write port of the VRAMs are synchronous to the IMS G201 processor clock (**Clk**). The timings of these strobes vary continuously depending on the contents of memory configuration register 1.

Figure 22.28 shows a basic read and write cycle to the VRAMs. Read data from the VRAM is latched into the IMS G201 using either **notVCAS0-1** or **notVOE**, whichever becomes inactive first. This varies depending on the memory parameters, see Table 22.20.

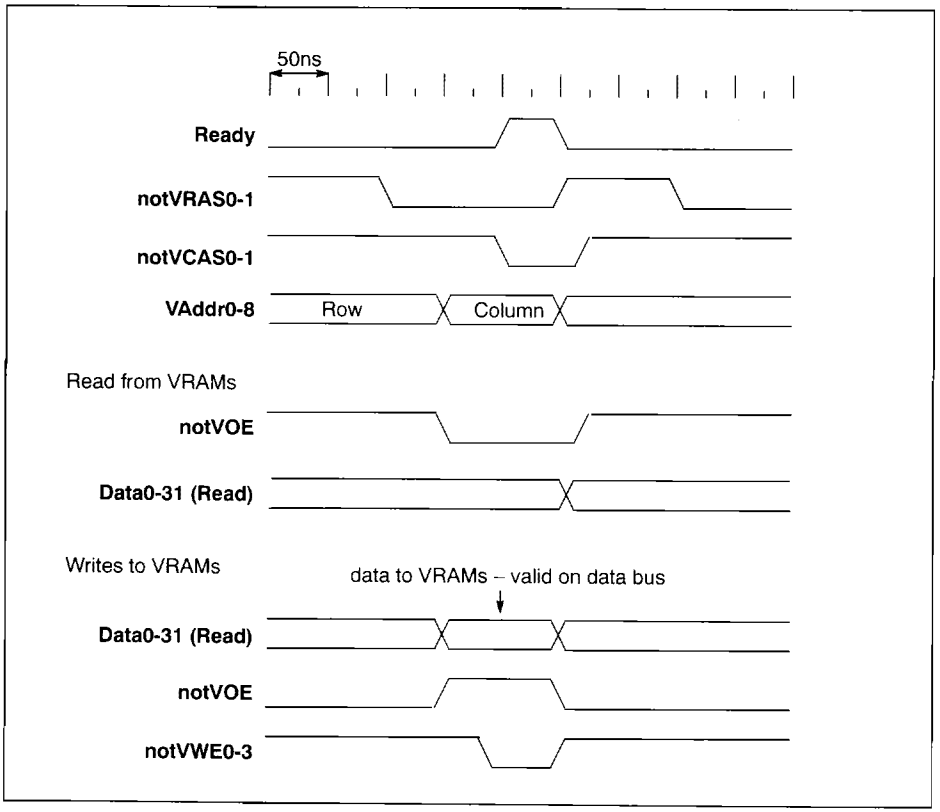

Figure 22.28 Basic memory controller access to VRAMs

Figure 22.29 shows the timings for basic multicycle accesses, alternatively referred to as page mode accesses.

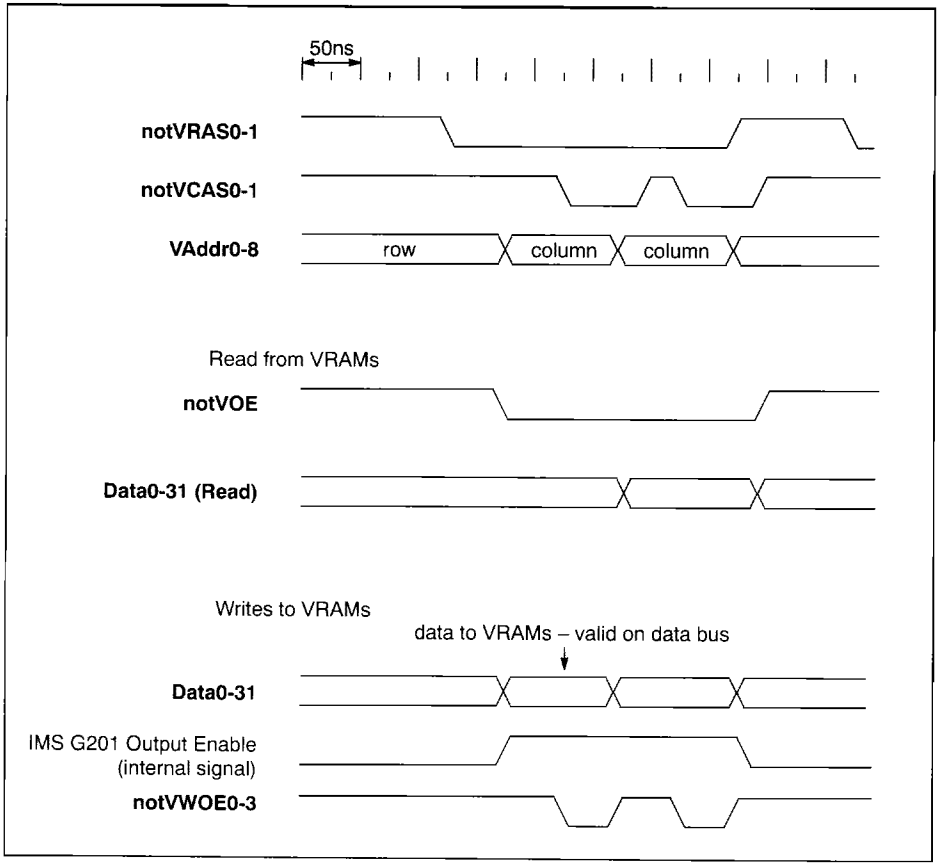

Figure 22.29 Memory controller access to VRAMs-multi cycle

Effects of setting the IMS G201 memory configuration registers

The timings of the VRAM cycles under various modes is dependent on the settings of the memory configuration register (index 01).

All bits marked '–' are reserved and must be masked out on reads and written to 0 (low) on writes unless otherwise specified.

Memory configuration 1 register (Index: 01)

7	6	5	4	3	2	1	0
–	–	–	–	–	RA	RP	VA

The previous two timing diagrams, Figures 22.28 and 22.29, showed the default timing with RA, RP and VA set to 0. Setting these bits to a value other than 0 will extend the VRAM cycles as indicated in the following table and timing diagrams.

Bit name	Bit	Definition
VA	0	When set to 1 it extends CAS and RAS active time for VRAM cycles, except refresh cycles. This parameter determines the nominal time from CAS falling to the next CAS falling during page cycles. Nominal CAS times are given below: When VA set to 0: CAS low time = 62.5ns CAS high time = 37.5ns CAS falling to CAS falling = 100ns Refresh falling to CAS falling lowtime = 112.5ns or 162.5ns When VA set to 1: CAS low time = 100ns CAS high time = 50ns CAS falling to CAS falling = 150ns Refresh falling to CAS falling lowtime = 100ns or 150ns
RP	1	When set to 1 it extends RAS precharge time between consecutive VRAM cycles by 25ns. This parameter extends the nominal time from RAS falling to the next RAS falling by 50ns. Nominal RAS times are given below: When RP set to 0: RAS falling to RAS falling = 250ns (5 clock cycles) Refresh falling to RAS falling = 200ns When RP set to 1: RAS falling to RAS falling = 300ns (6 clock cycles) Refresh falling to RAS falling = 250ns **Note**: If both VA and RP are set to 1 then RAS falling to RAS falling = 350ns (7 clock cycles).
RA	2	When set to 1 it extends CAS and RAS active time for VRAM refresh cycles. This parameter determines the nominal time that CAS and RAS are active during a refresh cycle to the VRAM. Nominal CAS/RAS times are given below: When RA set to 0: CAS/RAS low time = 100ns When RA set to 1: CAS/RAS low time = 150ns

Table 22.20 Effects of setting the Memory configuration 1 register

Bit 1 (RP) determines the time between cycles. If set to 1 the **notVRAS0-1** low and high times are each extended by half a cycle. If set to 0 RAS would be high for a nominal time of 100ns.

Bit 2 (RA) only affects refresh cycles which are described on page 545.

Random cycles

The read data from the VRAM is latched into the IMS G201 using either **notVCAS0-1** or **notVOE** whichever becomes inactive first. This varies depending on the setting of the memory parameters. Figure 22.30 gives the cycle timings for various settings of the Memory configuration 1 register.

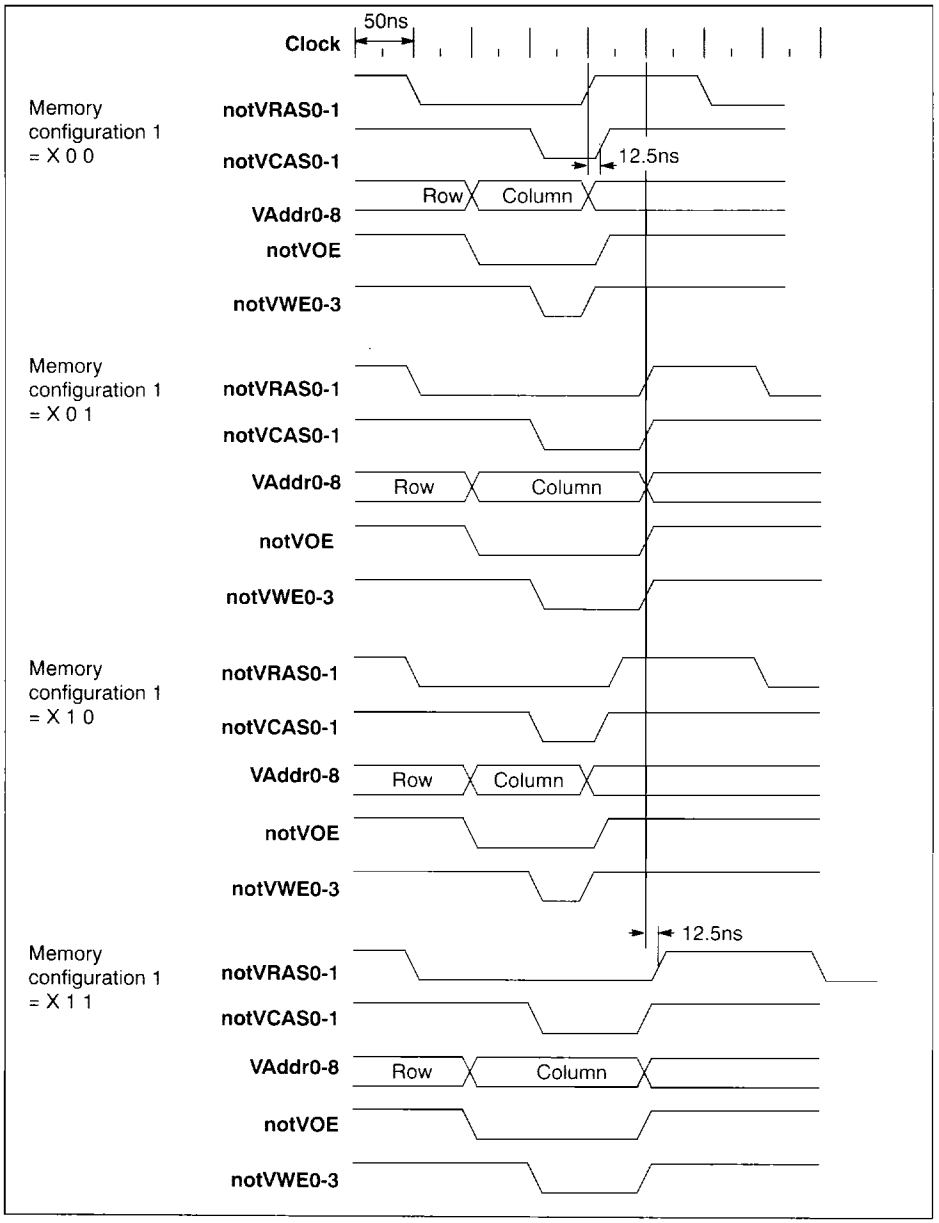

Figure 22.30 Random cycles -32 bit wide VRAMs for different Memory configuration 1 settings

Page mode cycles

Page mode cycles can occur for one of two reasons; either because the VRAM width does not enable the access to take place in one normal access (i.e. the VRAM width is less than 32 bits), or because the IMS G201 flags that there will be a paged mode access.

Figure 22.31 shows page mode cycle timings for different register settings.

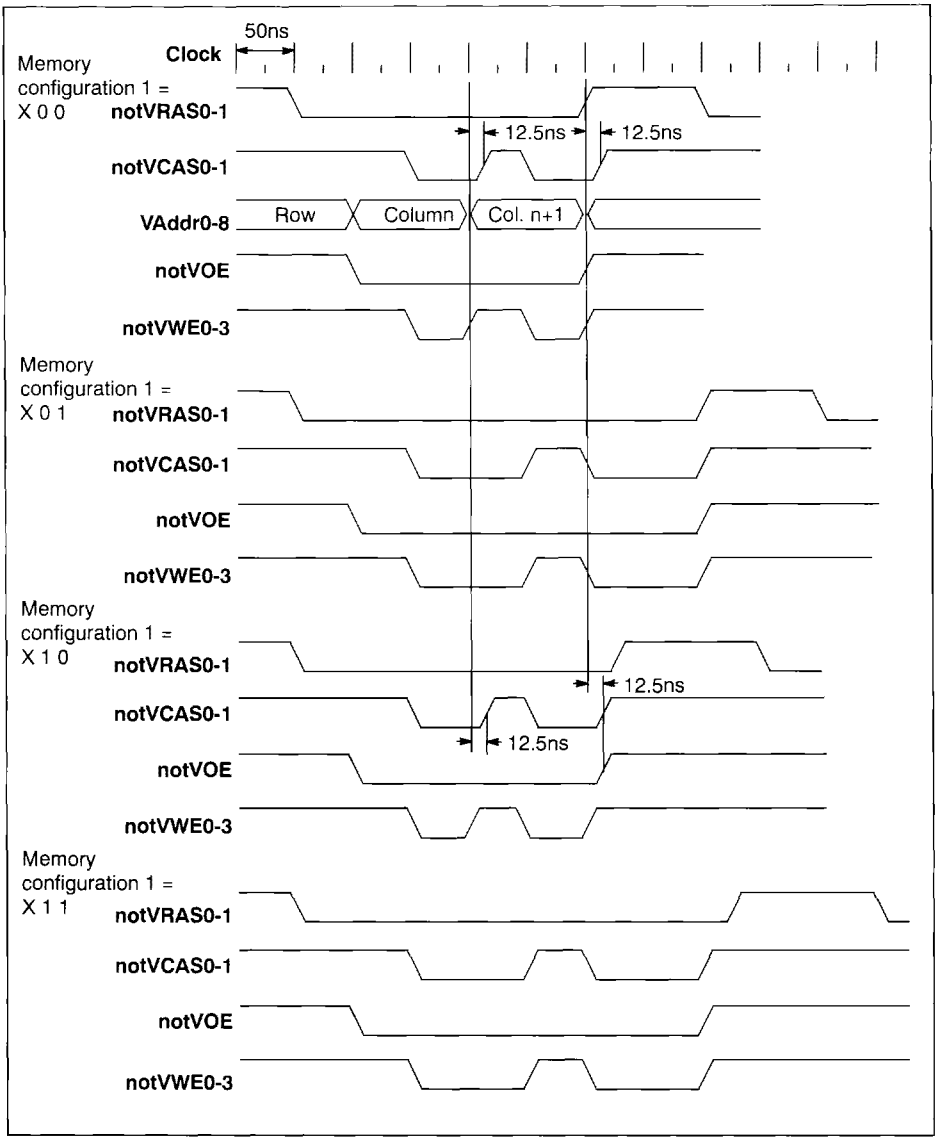

Figure 22.31 Page mode cycles - for different Memory configuration 1 settings

Refresh cycles

A CAS-before-RAS refresh cycle is used to refresh the VRAMs. The cycle can be extended by setting memory parameter index 1 (bit 3), thus extending the RAS/CAS active time by 50ns. The following diagram shows the timings for different settings of the **memory configuration 1** register (index 1).

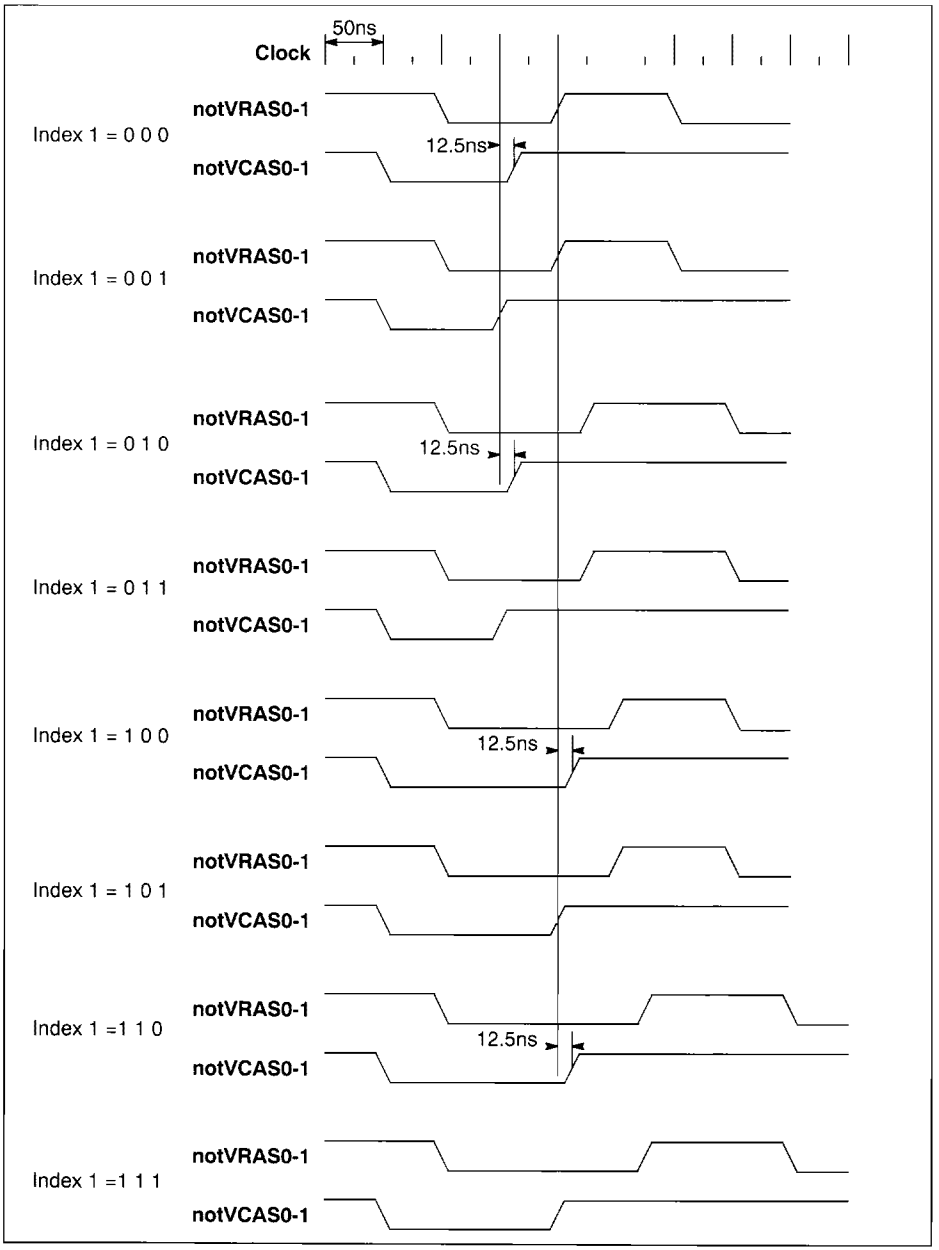

Figure 22.32 Refresh cycle timings for different settings of Memory configuration 1 register

Referencing of VRAM timings to the IMS G201 processor clock

As stated previously, all accesses on the random read/write port of the VRAMs are timed by and synchronous to the IMS G201 processor clock (**Clk**). Table 22.21 gives the absolute position of these strobes with respect to this clock.

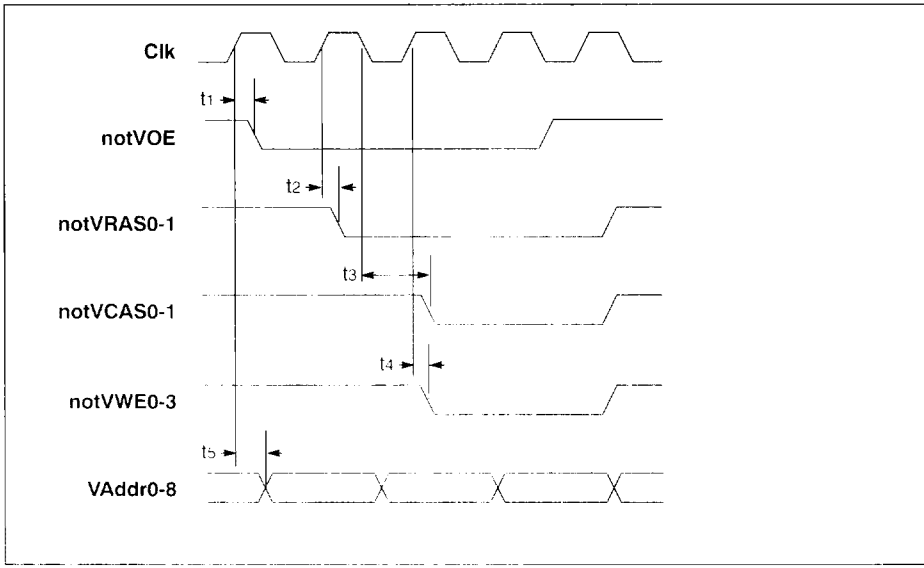

Figure 22.33 Referencing of VRAM timings to the IMS G201 processor clock

Symbol	Parameter	Min	Max	Unit	Notes
t1	**Clk** to **notVOE**	10	45	ns	
t2	**Clk** to **notVRAS0-1**	10	38	ns	
t3	**Clk** to **notVCAS0-1**	10	30	ns	
t4	**Clk** to **notVWE0-3**	10	20	ns	
t5	**Clk** to **VAddr0-8**	10	50	ns	

Table 22.21 VRAM timings

Transfer cycle timings

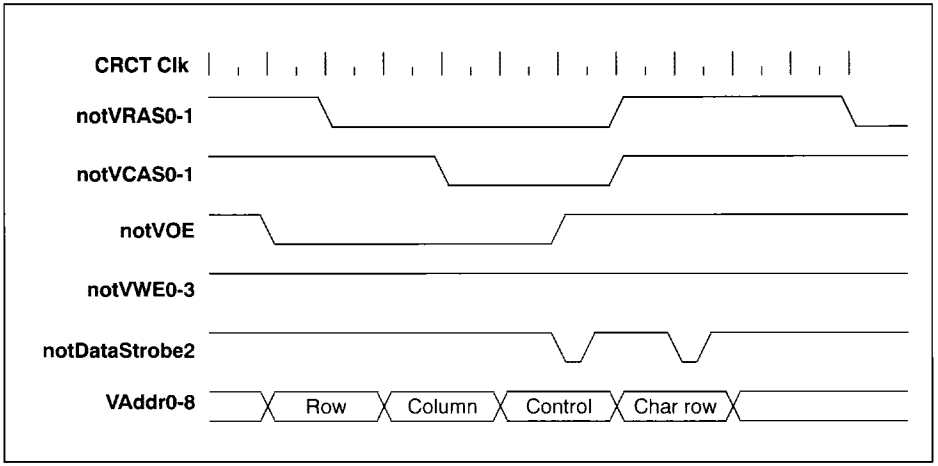

Figure 22.34 SAM load timing – basic transfer cycle

VRAM serial port interface timings

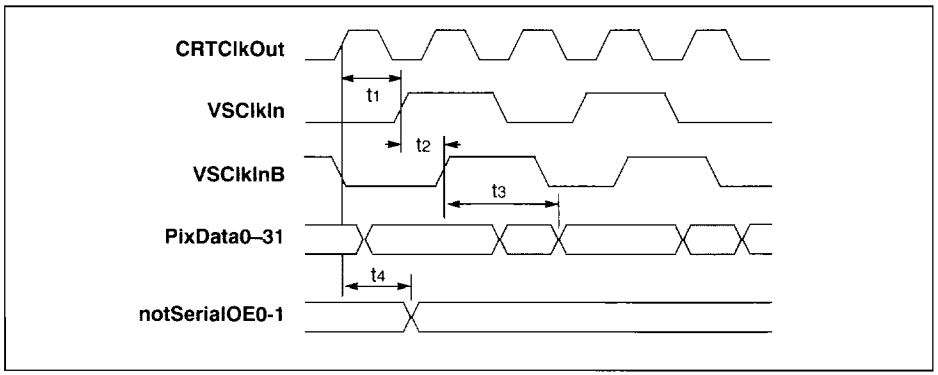

Figure 22.35 VRAM serial port interface timings diagram (see note 1, Table 22.22)

Symbol	Parameter	Min	Max	Units	Notes
t_1	**CRTClkOut** high to **VSClkIn** high	-	25.6	ns	1
t_2	On-card buffer delay	-	7.0	ns	1
t_3	VRAM access time	-	35.0	ns	1
t_4	IMS G191 **CRTClkOut** to IMS G201 **notSerialOE0-1**	-	28.0	ns	1

Note:
1 **CRTClkOut**, **VSClkIn**, **VSClkInB** and **PixData0-31** refer to IMS G191 pins

Table 22.22 VRAM serial port interface timings

22.12.3 IMS G191 interface timings

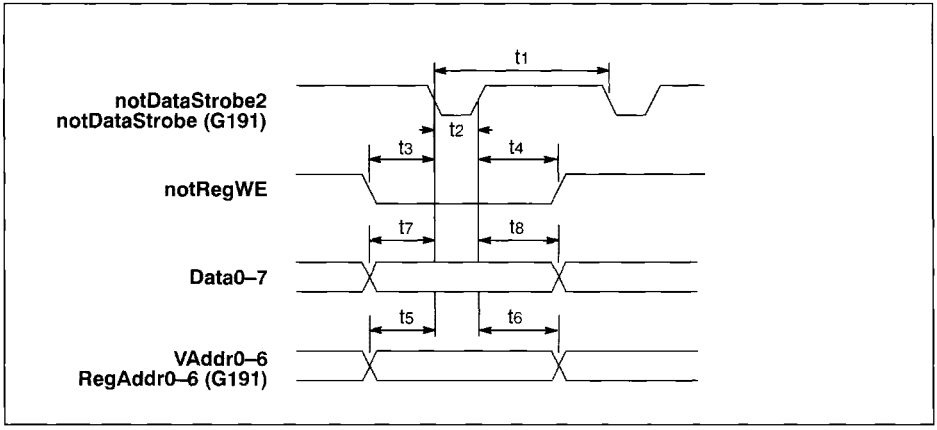

Figure 22.36 Write to IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe2** period - fast access	250.0		ns	
	notDataStrobe2 period - slow access	500.0		ns	
	notDataStrobe2 period - control codes	40.0		ns	
t2	**notDataStrobe2** width - fast access	100.0		ns	
	notDataStrobe2 width - slow access	150.0		ns	
	notDataStrobe2 width - control codes	20.0		ns	
t3	**notRegWE** set up to **notDataStrobe2**	50.0		ns	
t4	**notRegWE** hold after **notDataStrobe2**	40.0		ns	
t5	**VAddr0-6** set up to **notDataStrobe2**	40.0		ns	
t6	**VAddr0-6** hold after **notDataStrobe2**	40.0		ns	
t7	**Data0-7** set up to **notDataStrobe2**	40.0		ns	
t8	**Data0-7** hold after **notDataStrobe2**	40.0		ns	

Table 22.23 Write to IMS G191 register timings

Read from G191 register timings

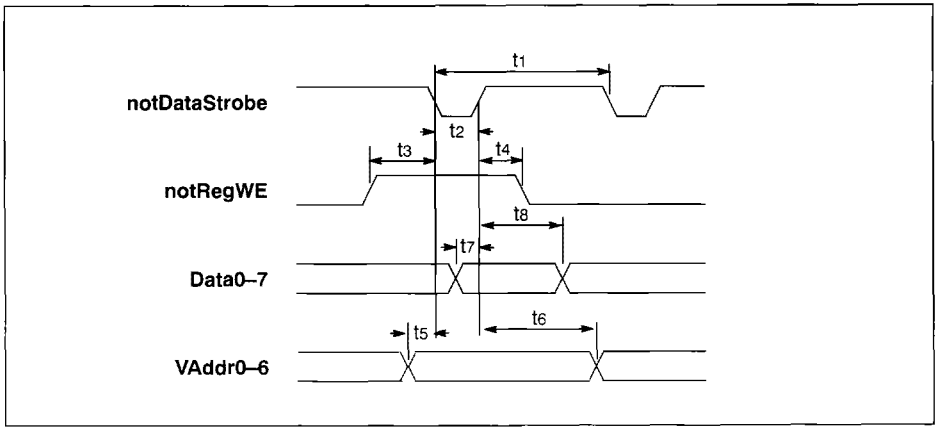

Figure 22.37 Read from IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe2** period - fast access	250.0		ns	
	notDataStrobe2 period - slow access	500.0		ns	
t2	**notDataStrobe2** width - fast access	100.0		ns	
	notDataStrobe2 width - slow access	150.0		ns	
t3	**notRegWE** set up to **notDataStrobe2**	40.0		ns	
t4	**notRegWE** hold after **notDataStrobe2**	40.0		ns	
t5	**VAddr0-6** setup to **notDataStrobe2**	40.0		ns	
t6	**VAddr0-6** hold after **notDataStrobe2**	40.0		ns	
t7	**Data0-7** read setup	40.0		ns	
t8	**Data0-7** hold after **notDataStrobe2**	0.0		ns	

Table 22.24 Read from IMS G191 register timings

22.12.4 CRT controller timings

CRTC clock timings

The CRTC clocks are generated by the IMS G191 and used by the IMS G201 to provide synchronization of signals between the IMS G201, VRAM and the IMS G191. Their frequency is set by bit 0 of the clock frequency select register.

The interface timing requirements of the clocks are given below. **CRTClkIn2** is half the frequency of **CRTClkIn**.

Video control timings

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G201 from the CRTC clocks and fed back into the IMS G191 via the **VideoCtrlIn0-1** pins.

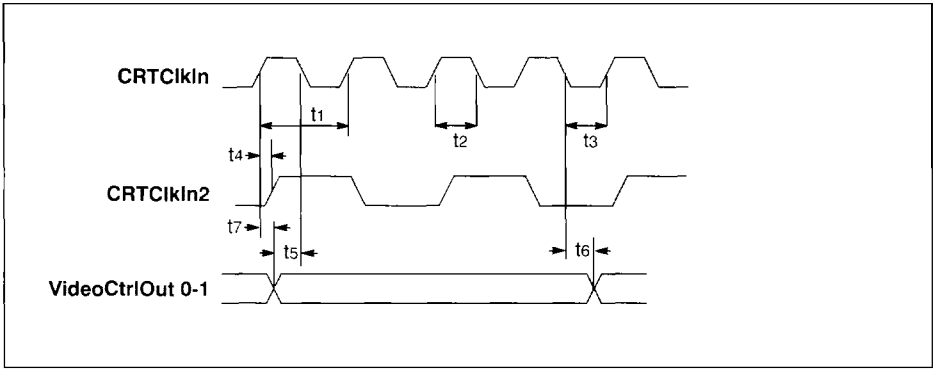

Figure 22.38 CRTC clock and video control timings

Symbol	Parameter	Min	Max	Units	Notes
t1	IMS G191 **CRTClkIn** period	22.0	50.0	ns	
t2	IMS G191 **CRTClkIn** pulse width high	8.0	32.0	ns	
t3	IMS G191 **CRTClkIn** pulse width low	8.0	32.0	ns	
t4	IMS G191 **CRTClkIn** to **CRTClkIn2** delay	−5.0	5.0	ns	
t5	**VideoCtrlOut0-1** setup time	5.0	–	ns	
t6	**VideoCtrlOut0-1** hold time	12.5	–	ns	
t7	IMS G191 **CRTClkIn** to **VideoCtrlOut0-1**		30.0	ns	

Table 22.25 CRTC clock timings

22.12.5 External memory timings for AT bus

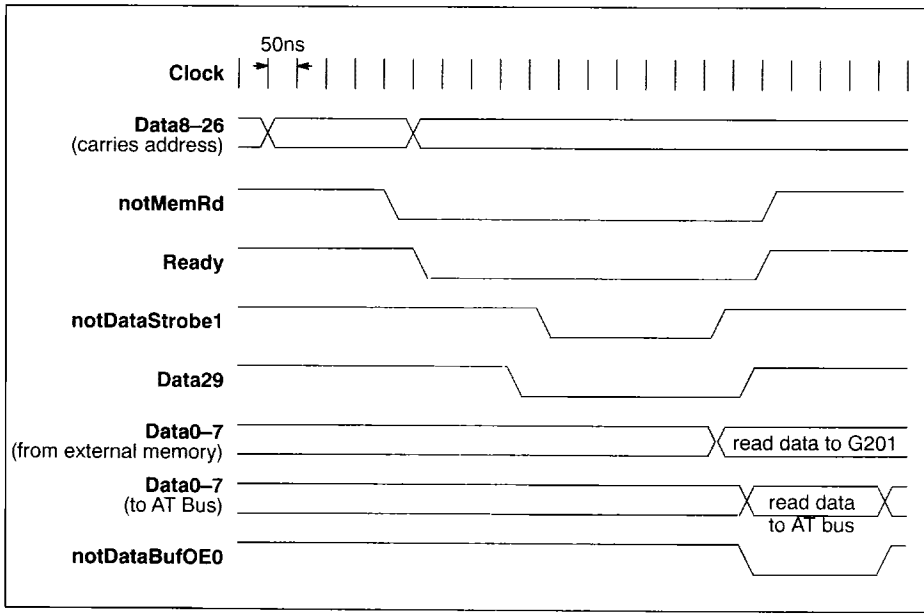

Figure 22.39 Read from external memory

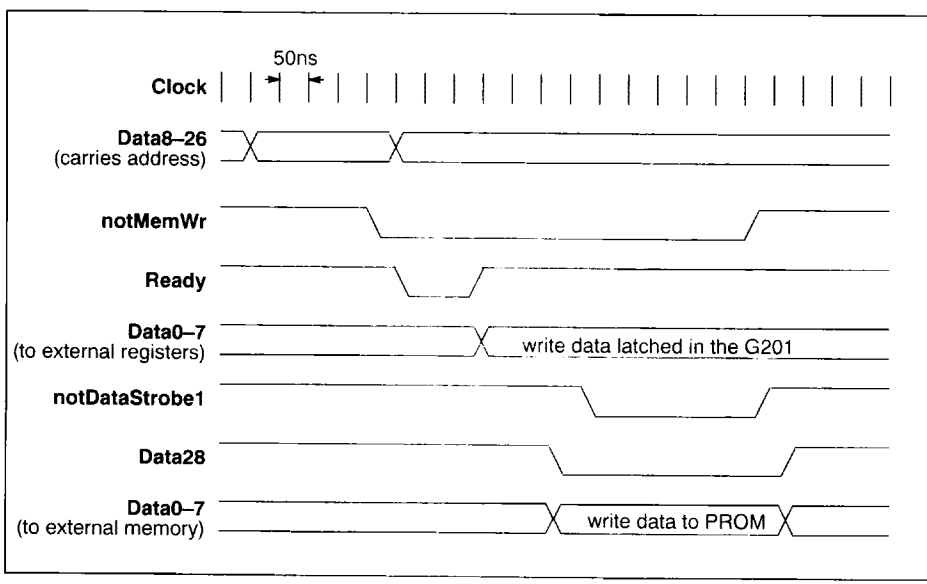

Figure 22.40 Write to external memory

22.12.6 External register timings for AT bus

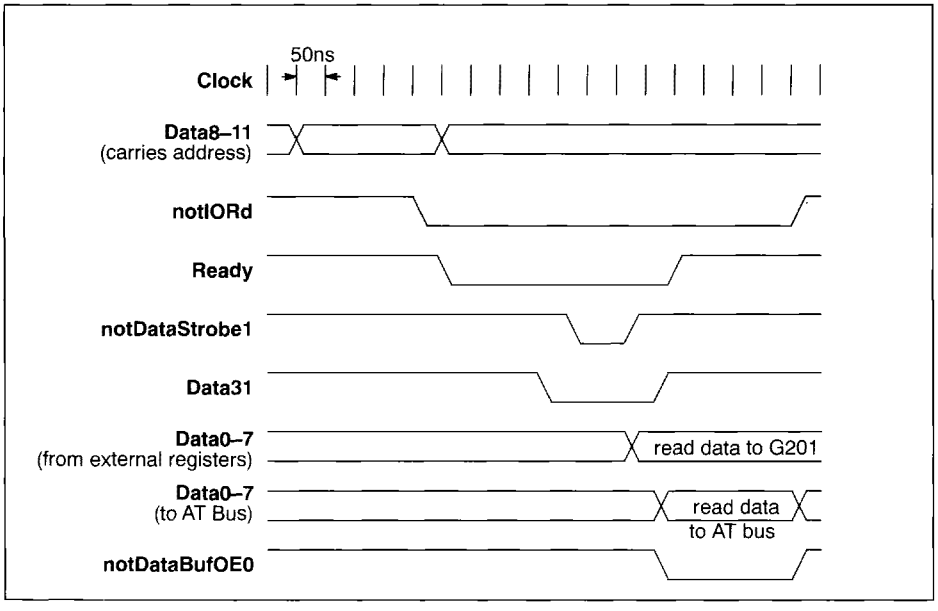

Figure 22.41 Read from external register

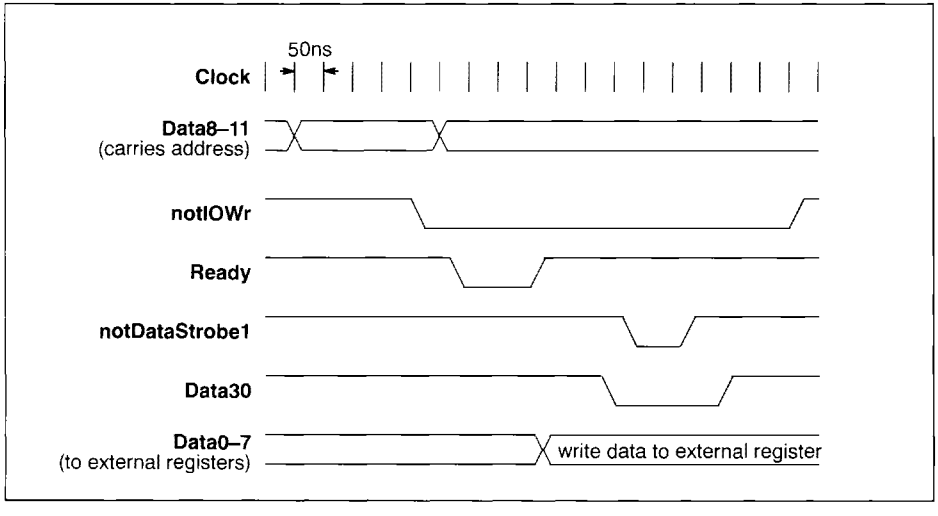

Figure 22.42 Write to external register

22.12.7 External memory timings for Micro Channel

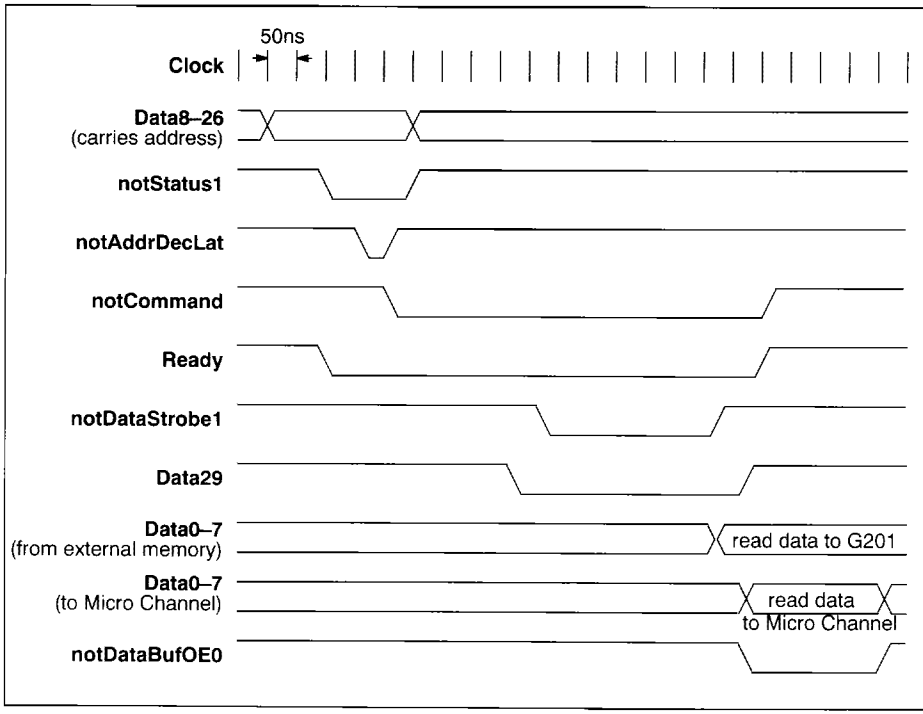

Figure 22.43 Read from external memory

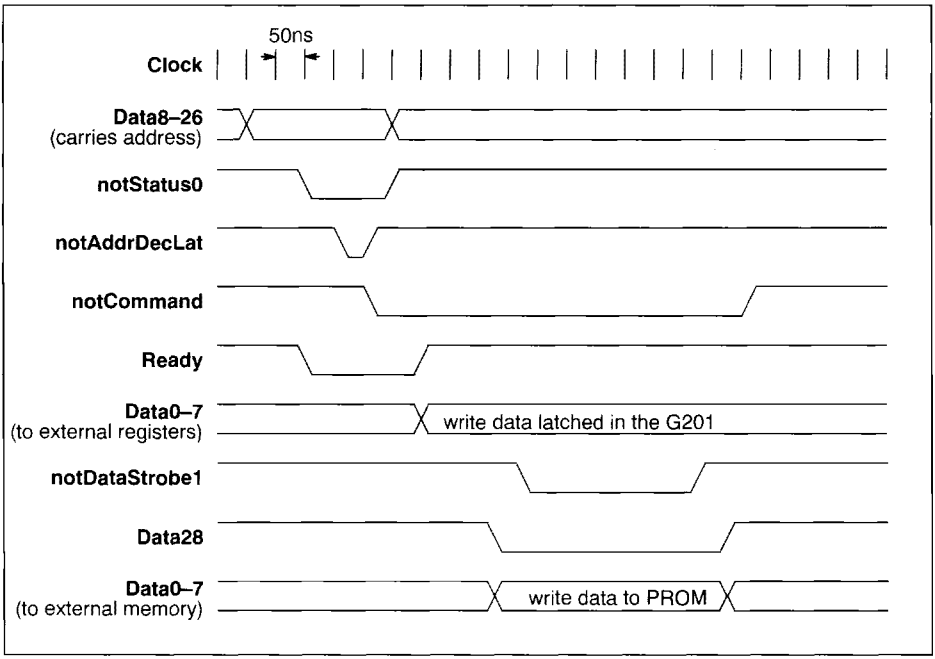

Figure 22.44 Write to external memory

22.12.8 External register timings for Micro Channel

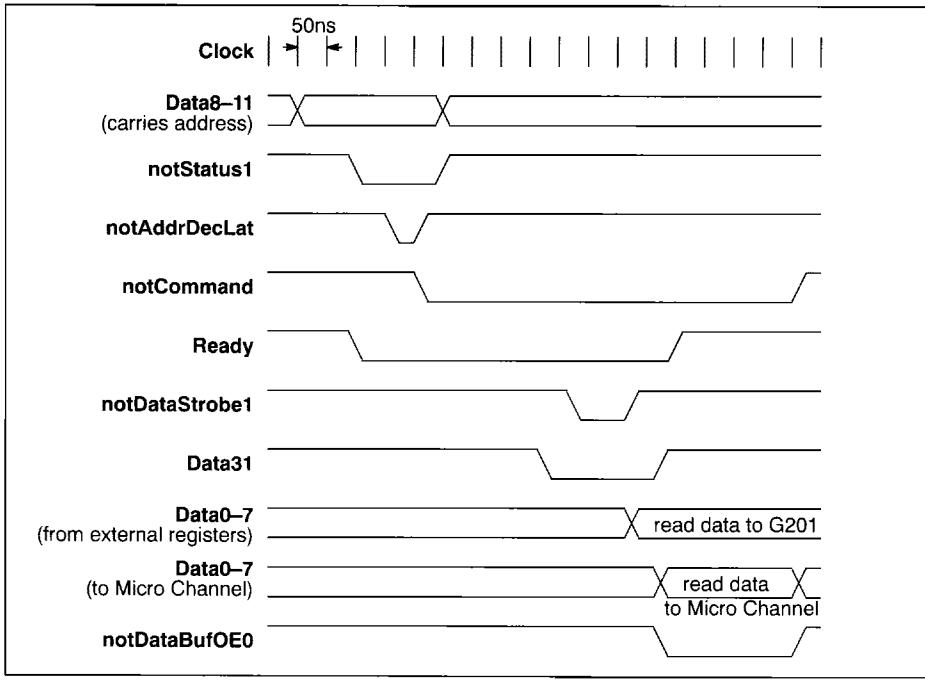

Figure 22.45 Read from external register

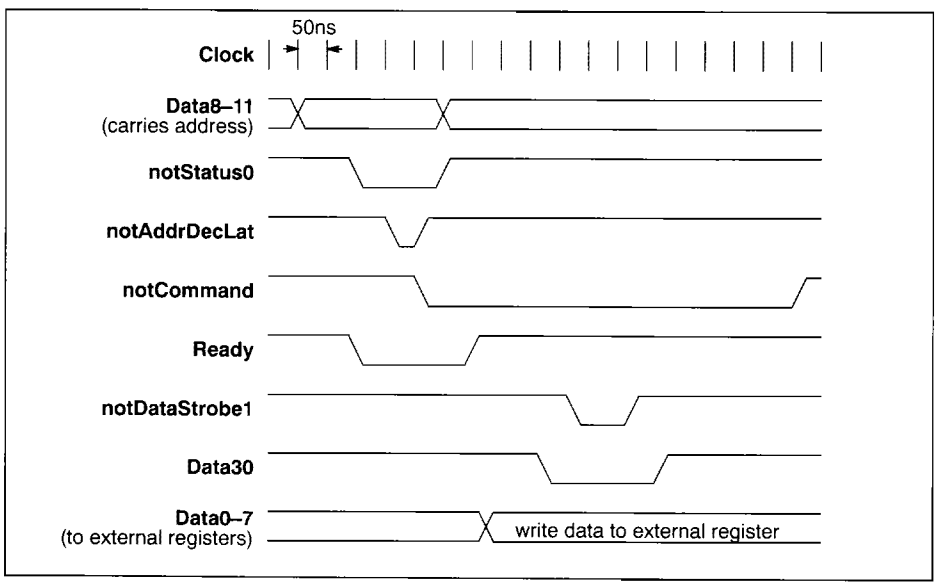

Figure 22.46 Write to external register

22.12.9 Reset timings

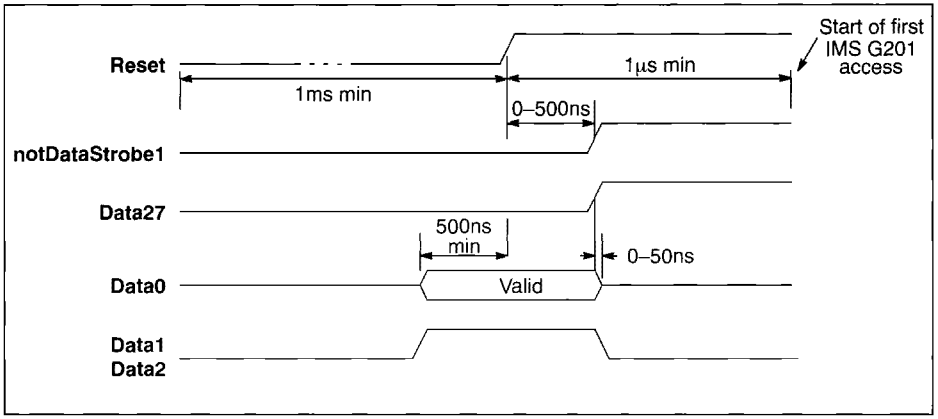

Figure 22.47 Reset timings

22.13 Electrical specifications

22.13.1 Absolute Maximum Ratings

Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply Voltage	0.0	7.5	Volts
V_I	Voltage on input pin	–1.0	V_{DD}+0.5	Volts
V_O	Voltage on output pin	–1.0	V_{DD}+0.5	Volts
T_S	Storage temperature	–65	150	°C
T_A	Temperature under bias	–55	125	°C

Table 22.26 Absolute maximum ratings

22.13.2 DC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply Voltage	4.5	5.5	Volts
T_A	Temperature under bias	0	70	°C
PD	Power dissipation		2	Watts
V_{IH}	Input logic '1' voltage	2.1	V_{DD}+0.5	Volts
V_{IL}	Input logic '0' voltage	–0.5	0.8	Volts
I_{IN}	Digital input current	–10	+10	μA

Table 22.27 DC operating conditions

Worst case timings are applicable only if the device is within the recommended parameters.

22.13.3 Pin output loading characteristics

AT bus mode

Pin name	C_L (pF)	V_{OH} (Volts)		V_{OL} (Volts)		I_{OH} (mA)	I_{OL} (mA)	R_S (Ω)		I_{slew}
	Max	Min	Max	Min	Max	Max	Max	Min	Max	Min
notMaster notCoProcStatOE15	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
notSerialOE0-1	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notIRQ notDataBufOE0-1 CoProcStat	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notIOCardSel16 notMemCardSel16	90	2.4	4.5	0.0	0.5	–1.3	24.0	–	–	–
VideoCtrlOut0-1 notDataStrobe2	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
MonHSync	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
Addr0-19 UnLatAddr17-23	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Medium
notSysByteHiEn	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Slow
DmaReq5-7 notMemWr notMemRd	240	2.4	4.5	0.0	0.5	–1.3	24.0	–	–	–
notCoProcStatOE7	17	2.4	4.5	0.0	0.5	–1.3	24.0	–	–	–
notVRAS0-1	24	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notVWE0-3	28	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notVCAS0-1 notVOE	28	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
VAddr0-8	33	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
VSClkOut	36	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
Ready	40	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
notDataStrobe1 AddrBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
DataBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
Data0-7	85	2.4	4.5	0.0	0.4	–0.7	8.0	20	30	Fast
Data8-31	85	2.4	4.5	0.0	0.4	–0.7	8.0	20	30	Medium
MonVSync	168	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow

Table 22.28 Pin output loading characteristics - AT bus mode

Where:

C_L is the maximum load capacitance
V_{OH} is the high level output voltage
V_{OL} is the low level output voltage
I_{OH} is the high level output current
I_{OL} is the low level output current
R_S is the termination impedance
I_{slew} is the current slew rate

Micro Channel bus mode

Pin name	C_L (pF)	V_{OH} (Volts)		V_{OL} (Volts)		I_{OH} (mA)	I_{OL} (mA)	R_S (Ω)		I_{slew}
	Max	Min	Max	Min	Max	Max	Max	Min	Max	Min
notBurst ArbOut0-3 notIRQ notDataBufOE0-3 CoProcStat	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notSerialOE0-1	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notPreemptOut notCoProcStatOE	17	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
notCardSelFbk notByteEn0-3 MemnotIO notCommand MemAddrEn24	240	2.4	4.5	0.0	0.5	–1.3	24.0	–	–	–
VideoCtrlOut0-1 notDataStrobe2	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
MonHSync	22	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notStatus0-1	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
Addr0-31	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Medium
notSysByteHiEn	24	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Slow
notAddrDecLat	24	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
notVRAS0-1	24	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
notVCAS0-1 notVOE	28	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
notVWE0-3	28	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Medium
notStrDatStb	33	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
VAddr0-8	33	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
VSClkOut	36	2.4	4.5	0.0	0.4	–1.5	4.0	40	50	Fast
Ready	40	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
notDataStrobe1 AddrBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow
DataBufDir	44	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Fast
Data0-7	85	2.4	4.5	0.0	0.4	–0.7	8.0	20	30	Fast
Data8-31	85	2.4	4.5	0.0	0.4	–0.7	8.0	20	30	Medium
MonVSync	168	2.4	4.5	0.0	0.4	–0.7	8.0	40	50	Slow

Table 22.29 Pin output loading characteristics - Micro Channel bus mode

Where:

C_L is the maximum load capacitance
V_{OH} is the high level output voltage
V_{OL} is the low level output voltage
I_{OH} is the high level output current
I_{OL} is the low level output current
R_S is the termination impedance
I_{slew} is the current slew rate

22.14 Package specifications

22.14.1 208 pin plastic flat pack package dimensions

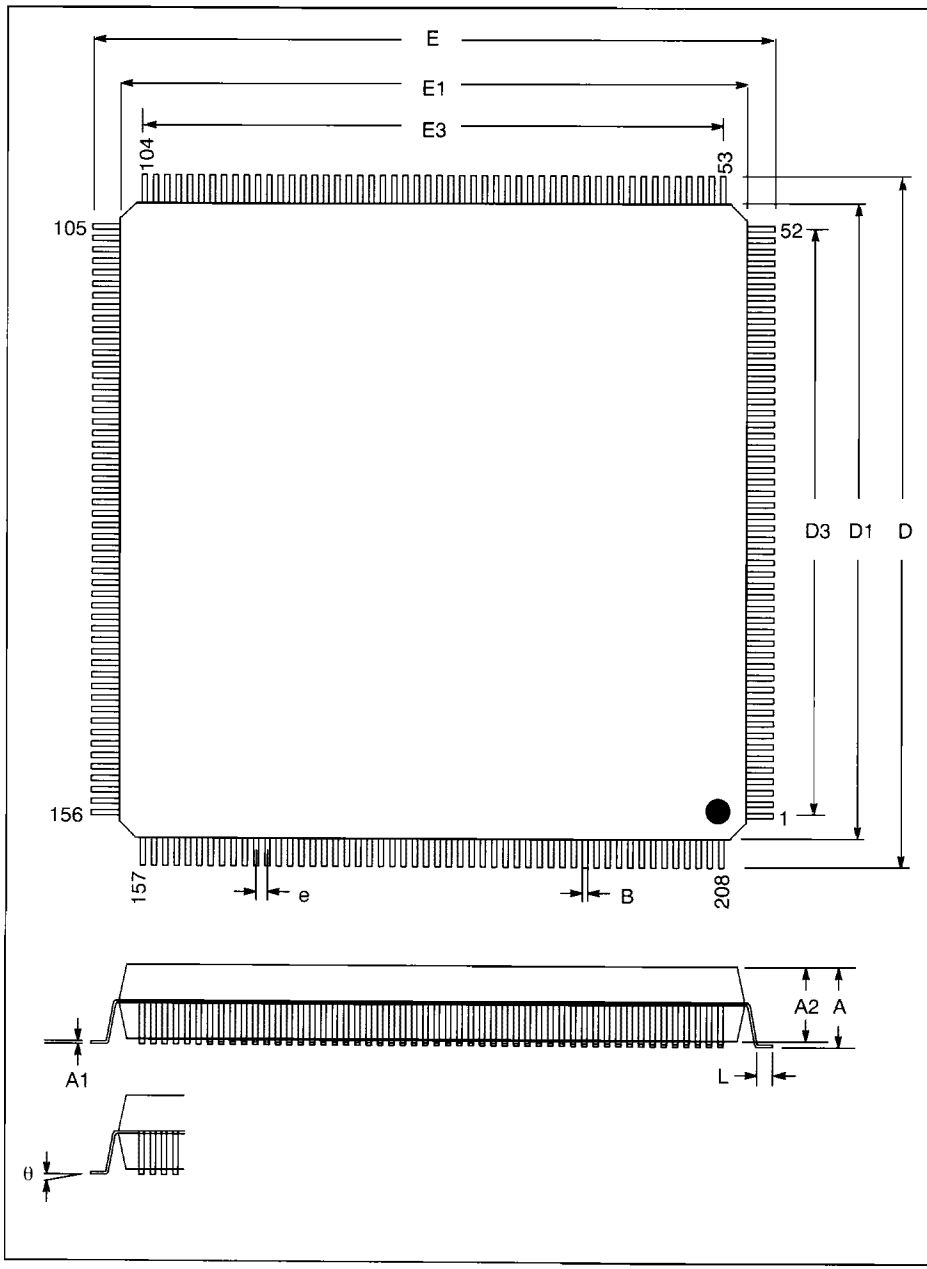

Figure 22.48 208 lead plastic quad flat pack

DIM	Millimeters			Inches			Notes
	MIN	NOM	MAX	MIN	NOM	MAX	
A			4.200			0.165	
A_1	0.120	0.160	0.200	0.0047	0.0063	0.0079	
A_2		3.40			0.134		Ref.
D	30.40	30.60	30.80	1.197	1.205	1.213	
D_1	27.80	28.00	28.20	1.094	1.102	1.110	
E	30.40	30.60	30.80	1.197	1.205	1.213	
E1	27.80	28.00	28.20	1.094	1.102	1.110	
L	0.400	0.500	0.600	0.016	0.02	0.024	
e		0.50			0.02		BSC
B	0.180	0.230	0.280	0.007	0.009	0.011	
θ		0°	5°				

Table 22.30 208 lead plastic quad flat pack

22.14.2 IMS G201 AT bus package pinout

208 pin plastic quad flatpack package

The IMS G201 AT bus package pinout referenced by pin number is given in Table 22.31. The IMS G201 AT bus package pinout referenced by signal name is given in Table 22.32.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD	53	notMemCardSel16	105	VDD	157	HoldToVDD
2	GND	54	HoldToVDD	106	GND	158	N/C
3	DataBufDir	55	VDD	107	CRTClkIn	159	HoldToGND
4	notDataBufOE0	56	GND	108	CRTClkIn2	160	HoldToGND
5	notDataBufOE1	57	Addr0	109	Clk	161	VDD
6	N/C	58	Addr1	110	VideoCtrlOut0	162	GND
7	N/C	59	Addr2	111	VideoCtrlOut1	163	Data31
8	VDD	60	Addr3	112	VDD	164	Data30
9	GND	61	Addr4	113	GND	165	Data29
10	N/C	62	VDD	114	VSClkOut	166	VDD
11	N/C	63	GND	115	notSerialOE0	167	GND
12	notSysMemWr	64	Addr5	116	notSerialOE1	168	Data28
13	N/C	65	Addr6	117	notDataStrobe1	169	Data27
14	notSysByteHiEn	66	Addr7	118	notDataStrobe2	170	Data26
15	notRefresh	67	Addr8	119	MonVSync	171	Data25
16	AddrEn	68	Addr9	120	MonHSync	172	Data24
17	notSysMemRd	69	Addr10	121	N/C	173	Data23
18	GND	70	GND	122	N/C	174	GND
19	N/C	71	Addr11	123	N/C	175	Data22
20	Reset	72	Addr12	124	GND	176	Data21
21	notIOCardSel16	73	Addr13	125	VAddr8	177	Data20
22	Ready	74	Addr14	126	VAddr7	178	Data19
23	N/C	75	Addr15	127	VAddr6	179	Data18
24	notMemRd	76	Addr16	128	VAddr5	180	Data17
25	notMemWr	77	Addr17	129	VAddr4	181	Data16
26	VDD	78	VDD	130	VDD	182	VDD
27	GND	79	GND	131	GND	183	GND
28	notIORd	80	Addr18	132	VAddr3	184	Data15
29	notIOWr	81	Addr19	133	VAddr2	185	Data14
30	notChannelCheck	82	Addr20	134	VAddr1	186	Data13
31	notDmaAck5	83	UnLatAddr21	135	VAddr0	187	Data12
32	N/C	84	UnLatAddr22	136	GND	188	Data11
33	DmaReq3	85	UnLatAddr23	137	notVWE3	189	Data10
34	N/C	86	UnLatAddr17	138	notVWE2	190	Data9
35	GND	87	GND	139	notVWE1	191	GND
36	DmaReq2	88	UnLatAddr18	140	notVWE0	192	Data8
37	N/C	89	UnLatAddr19	141	N/C	193	Data7
38	DmaReq1	90	notDmaAck0	142	notVOE	194	Data6
39	N/C	91	notDmaAck1	143	N/C	195	Data5
40	DmaReq0	92	notDmaAck2	144	N/C	196	Data4
41	notIRQ	93	notDmaAck3	145	notVCAS1	197	Data3
42	N/C	94	VDD	146	notVCAS0	198	VDD
43	notMaster	95	GND	147	N/C	199	GND
44	VDD	96	notDmaAck7	148	VDD	200	Data2
45	GND	97	DmaReq5	149	GND	201	Data1
46	notDmaAck6	98	DmaReq6	150	N/C	202	Data0
47	BusAddrLatEn	99	DmaReq7	151	notVRAS1	203	VDD
48	N/C	100	notCoProcStatOE7	152	notVRAS0	204	GND
49	MonSyncOE	101	VDD	153	GND	205	notCoProcStatOE15
50	AddrBufDir	102	GND	154	N/C	206	CoProcStat
51	VDD	103	N/C	155	N/C	207	HoldToGND
52	GND	104	N/C	156	N/C	208	HoldToGND

Table 22.31 208 pin package pinout by pin number for **AT bus mode**

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
Addr0	57	Data17	180	N/C	6	notSysByteHiEn	14
Addr1	58	Data18	179	N/C	7	notSysMemRd	17
Addr2	59	Data19	178	N/C	10	notSysMemWr	12
Addr3	60	Data20	177	N/C	11	notVCAS0	146
Addr4	61	Data21	176	N/C	13	notVCAS1	145
Addr5	64	Data22	175	N/C	19	notVOE	142
Addr6	65	Data23	173	N/C	23	notVRAS0	152
Addr7	66	Data24	172	N/C	32	notVRAS1	151
Addr8	67	Data25	171	N/C	34	notVWE0	140
Addr9	68	Data26	170	N/C	37	notVWE1	139
Addr10	69	Data27	169	N/C	39	notVWE2	138
Addr11	71	Data28	168	N/C	42	notVWE3	137
Addr12	72	Data29	165	N/C	48	Ready	22
Addr13	73	Data30	164	N/C	103	Reset	20
Addr14	74	Data31	163	N/C	104	UnLatAddr17	86
Addr15	75	GND	2	N/C	121	UnLatAddr18	88
Addr16	76	GND	9	N/C	122	UnLatAddr19	89
Addr17	77	GND	18	N/C	123	UnLatAddr20	82
Addr18	80	GND	27	N/C	141	UnLatAddr21	83
Addr19	81	GND	35	N/C	143	UnLatAddr22	84
AddrBufDir	50	GND	45	N/C	144	UnLatAddr23	85
AddrEn	16	GND	52	N/C	147	VAddr0	135
BusAddrLatEn	47	GND	56	N/C	150	VAddr1	134
Clk	109	GND	63	N/C	154	VAddr2	133
CoProcStat	206	GND	70	N/C	155	VAddr3	132
CRTClkIn	107	GND	79	N/C	156	VAddr4	129
CRTClkIn2	108	GND	87	N/C	158	VAddr5	128
DataBufDir	3	GND	95	notChannelCheck	30	VAddr6	127
DmaReq0	40	GND	102	notCoProcStatOE7	100	VAddr7	126
DmaReq1	38	GND	106	notCoProcStatOE15	205	VAddr8	125
DmaReq2	36	GND	113	notDataBufOE0	4	VDD	1
DmaReq3	33	GND	124	notDataBufOE1	5	VDD	8
DmaReq5	97	GND	131	notDataStrobe1	117	VDD	26
DmaReq6	98	GND	136	notDataStrobe2	118	VDD	44
DmaReq7	99	GND	149	notDmaAck0	90	VDD	51
Data0	202	GND	153	notDmaAck1	91	VDD	55
Data1	201	GND	162	notDmaAck2	92	VDD	62
Data2	200	GND	167	notDmaAck3	93	VDD	78
Data3	197	GND	174	notDmaAck5	31	VDD	94
Data4	196	GND	183	notDmaAck6	46	VDD	101
Data5	195	GND	191	notDmaAck7	96	VDD	105
Data6	194	GND	199	notIOCardSel16	21	VDD	112
Data7	193	GND	204	notIORd	28	VDD	130
Data8	192	HoldToGND	159	notIOWr	29	VDD	148
Data9	190	HoldToGND	160	notIRQ	41	VDD	161
Data10	189	HoldToGND	207	notMaster	43	VDD	166
Data11	188	HoldToGND	208	notMemCardSel16	53	VDD	182
Data12	187	HoldToVDD	54	notMemRd	24	VDD	198
Data13	186	HoldToVDD	157	notMemWr	25	VDD	203
Data14	185	MonHSync	120	notRefresh	15	VideoCtrlOut0	110
Data15	184	MonSyncOE	49	notSerialOE0	115	VideoCtrlOut1	111
Data16	181	MonVSync	119	notSerialOE1	116	VSClkOut	114

Table 22.32 IMS G201 208 pin PQFP **AT bus** pinout by signal name

22.14.3 IMS G201 Micro Channel bus package pinout

208 pin plastic quad flatpack package

The IMS G201 Micro Channel bus package pinout referenced by pin number is given in Table 22.33. The IMS G201 Micro Channel bus package pinout referenced by signal name is given in Table 22.34.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD	53	MemAddrEn24	105	VDD	157	HoldToVDD
2	GND	54	HoldToVDD	106	GND	158	N/C
3	DataBufDir	55	VDD	107	CRTClkIn	159	HoldToGND
4	notDataBufOE0	56	GND	108	CRTClkIn2	160	HoldToGND
5	notDataBufOE1	57	Addr0	109	Clk	161	VDD
6	notDataBufOE2	58	Addr1	110	VideoCtrlOut0	162	GND
7	notDataBufOE3	59	Addr2	111	VideoCtrlOut1	163	Data31
8	VDD	60	Addr3	112	VDD	164	Data30
9	GND	61	Addr4	113	GND	165	Data29
10	N/C	62	VDD	114	VSClkOut	166	VDD
11	notDSize32Rtn	63	GND	115	notSerialOE0	167	GND
12	notStrDatReq1	64	Addr5	116	notSerialOE1	168	Data28
13	N/C	65	Addr6	117	notDataStrobe1	169	Data27
14	notSysByteHiEn	66	Addr7	118	notDataStrobe2	170	Data26
15	notRefresh	67	Addr8	119	MonVSync	171	Data25
16	notDSize16Rtn	68	Addr9	120	MonHSync	172	Data24
17	notStrDatReq0	69	Addr10	121	N/C	173	Data23
18	GND	70	GND	122	N/C	174	GND
19	notStrDatStb	71	Addr11	123	N/C	175	Data22
20	Reset	72	Addr12	124	GND	176	Data21
21	notCardSelFbk	73	Addr13	125	VAddr8	177	Data20
22	Ready	74	Addr14	126	VAddr7	178	Data19
23	ReadyRtn	75	Addr15	127	VAddr6	179	Data18
24	notCommand	76	Addr16	128	VAddr5	180	Data17
25	MemnotIO	77	Addr17	129	VAddr4	181	Data16
26	VDD	78	VDD	130	VDD	182	VDD
27	GND	79	GND	131	GND	183	GND
28	notStatus1	80	Addr18	132	VAddr3	184	Data15
29	notStatus0	81	Addr19	133	VAddr2	185	Data14
30	notChannelCheck	82	Addr20	134	VAddr1	186	Data13
31	ArbGrant	83	Addr21	135	VAddr0	187	Data12
32	ArbOut3	84	Addr22	136	GND	188	Data11
33	ArbIn3	85	Addr23	137	notVWE3	189	Data10
34	ArbOut2	86	Addr24	138	notVWE2	190	Data9
35	GND	87	GND	139	notVWE1	191	GND
36	ArbIn2	88	Addr25	140	notVWE0	192	Data8
37	ArbOut1	89	Addr26	141	N/C	193	Data7
38	ArbIn1	90	Addr27	142	notVOE	194	Data6
39	ArbOut0	91	Addr28	143	N/C	195	Data5
40	ArbIn0	92	Addr29	144	N/C	196	Data4
41	notIRQ	93	Addr30	145	notVCAS1	197	Data3
42	notBurst	94	VDD	146	notVCAS0	198	VDD
43	notPreemptOut	95	GND	147	N/C	199	GND
44	VDD	96	Addr31	148	VDD	200	Data2
45	GND	97	notByteEn0	149	GND	201	Data1
46	notPreemptIn	98	notByteEn1	150	N/C	202	Data0
47	notAddrDecLat	99	notByteEn2	151	notVRAS1	203	VDD
48	N/C	100	notByteEn3	152	notVRAS0	204	GND
49	MonSyncOE	101	VDD	153	GND	205	notCoProcStatOE
50	AddrBufDir	102	GND	154	N/C	206	CoProcStat
51	VDD	103	N/C	155	N/C	207	HoldToGND
52	GND	104	N/C	156	N/C	208	HoldToGND

Table 22.33 208 pin package pinout by pin number for **Micro Channel bus mode**

Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin
Addr0	57	Data6	194	GND	191	notRefresh	15
Addr1	58	Data7	193	GND	199	notSerialOE0	115
Addr2	59	Data8	192	GND	204	notSerialOE1	116
Addr3	60	Data9	190	HoldToGND	159	notStatus0	29
Addr4	61	Data10	189	HoldToGND	160	notStatus1	28
Addr5	64	Data11	188	HoldToGND	207	notStrDatReq0	17
Addr6	65	Data12	187	HoldToGND	208	notStrDatReq1	12
Addr7	66	Data13	186	HoldToVDD	54	notStrDatStb	19
Addr8	67	Data14	185	HoldToVDD	157	notSysByteHiEn	14
Addr9	68	Data15	184	MemAddrEn24	53	notVCAS0	146
Addr10	69	Data16	181	MemnotIO	25	notVCAS1	145
Addr11	71	Data17	180	MonHSync	120	notVRAS1	151
Addr12	72	Data18	179	MonSyncOE	49	notVRAS0	152
Addr13	73	Data19	178	MonVSync	119	notVWE0	140
Addr14	74	Data20	177	N/C	10	notVWE1	139
Addr15	75	Data21	176	N/C	13	notVWE2	138
Addr16	76	Data22	175	N/C	48	notVWE3	137
Addr17	77	Data23	173	N/C	103	notVOE	142
Addr18	80	Data24	172	N/C	104	Ready	22
Addr19	81	Data25	171	N/C	121	ReadyRtn	23
Addr20	82	Data26	170	N/C	122	Reset	20
Addr21	83	Data27	169	N/C	123	VAddr0	135
Addr22	84	Data28	168	N/C	141	VAddr1	134
Addr23	85	Data29	165	N/C	143	VAddr2	133
Addr24	86	Data30	164	N/C	144	VAddr3	132
Addr25	88	Data31	163	N/C	147	VAddr4	129
Addr26	89	DataBufDir	3	N/C	150	VAddr5	128
Addr27	90	GND	2	N/C	154	VAddr6	127
Addr28	91	GND	9	N/C	155	VAddr7	126
Addr29	92	GND	18	N/C	156	VAddr8	125
Addr30	93	GND	27	N/C	158	VDD	1
Addr31	96	GND	35	notAddrDecLat	47	VDD	8
AddrBufDir	50	GND	45	notBurst	42	VDD	26
ArbGrant	31	GND	52	notByteEn0	97	VDD	44
ArbIn0	40	GND	56	notByteEn1	98	VDD	51
ArbIn1	38	GND	63	notByteEn2	99	VDD	55
ArbIn2	36	GND	70	notByteEn3	100	VDD	62
ArbIn3	33	GND	79	notCardSelFbk	21	VDD	78
ArbOut0	39	GND	87	notChannelCheck	30	VDD	94
ArbOut1	37	GND	95	notCommand	24	VDD	101
ArbOut2	34	GND	102	notCoProcStatOE	205	VDD	105
ArbOut3	32	GND	106	notDataBufOE0	4	VDD	112
Clk	109	GND	113	notDataBufOE1	5	VDD	130
CoProcStat	206	GND	124	notDataBufOE2	6	VDD	148
CRTClkIn	107	GND	131	notDataBufOE3	7	VDD	161
CRTClkIn2	108	GND	136	notDSize16Rtn	16	VDD	166
Data0	202	GND	149	notDSize32Rtn	11	VDD	182
Data1	201	GND	153	notDataStrobe1	117	VDD	198
Data2	200	GND	162	notDataStrobe2	118	VDD	203
Data3	197	GND	167	notIRQ	41	VideoCtrlOut0	110
Data4	196	GND	174	notPreemptIn	46	VideoCtrlOut1	111
Data5	195	GND	183	notPreemptOut	43	VSClkOut	114

Table 22.34 IMS G201 208 pin PQFP **Micro Channel bus** pinout by signal name

22.15 Ordering information

Device	Clock rate	Package	Part number
IMS G201	40MHz	208 pin plastic quad flat pack	IMS G201X-40S