TECHNICAL NOTE

UPGRADING FROM 1 MEG TO 2 MEG VRAMs

INTRODUCTION

Designers of VRAM-based graphics systems are now being presented with the opportunity to switch from 1 Meg to 2 Meg VRAMs. As with any move to higher density memory devices, this allows a system to be modified to either provide the same amount of total memory while using fewer devices, or to provide additional memory without increasing the number of devices used. When the total memory size remains the same, benefits include decreased board space due to fewer components, increased reliability due to fewer connections, and lower component cost when the cost-per-bit of the higher density components falls below that of the lower density components. An additional benefit of switching from 1 Meg to 2 Meg VRAMs is the availability of a more advanced feature set at the 2 Meg level.

Micron offers four versions of the 2 Meg VRAM; each addresses different user needs and each has different design requirements. When switching from 1 Meg VRAMs, the memory configuration, the required feature set and the board layout determine which version of the 2 Meg to switch to and the design effort involved. This article covers each of these three major areas of concern. In the area of memory configuration, the effects of specific factors on the design of the graphics memory controller are discussed. These factors include whether the 1 Meg VRAMs currently used are organized as x4 or as x8, the number of VRAM banks and whether or not the total memory size will be increased. In the area of feature sets, the different sets of functions available at the 2 Meg level are compared to the functions available at the 1 Meg level. Finally, in the area of physical layout, the different packages offered at the 1 Meg and 2 Meg levels are described.

MEMORY CONFIGURATION

Based on the memory configuration factors mentioned above, there are several possible scenarios when switching to 2 Meg VRAMs, ranging from straightforward intrabank replacement transparent to the graphics memory controller, to more involved memory expansion or interbank replacement; the latter two have controller implications. The following examples illustrate the different scenarios.

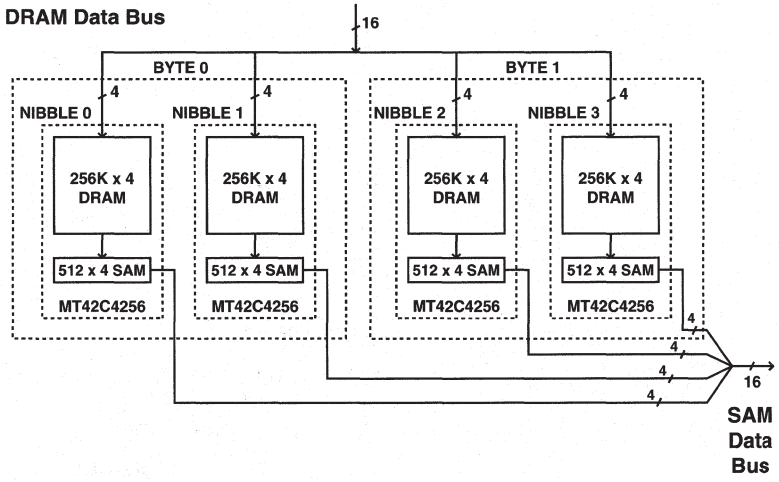


Figure 1
0.5 MB MEMORY ARRAY WITH A 16-BIT INTERFACE USING 1 MEG VRAMs

CASE 1: x4, 1 MEG VRAMS VS x8, 2 MEG VRAMs
Replacement of 4-bit-wide 1 Meg VRAMs with 8-bit-wide 2 Meg VRAMs is the most straightforward case when upgrading. This is illustrated in Examples 1 and 2.

Example 1
A 0.5 MB memory array implemented with a single bank of 4-bit-wide 1 Meg VRAMs (Micron's MT42C4256) is shown in Figure 1. The DRAM portion of the MT42C4256 is organized as 256K x 4, or 512 rows by 512 columns by 4 bits wide. The DRAM portion of 2 Meg VRAMs is organized as 256K x 8, or 512 rows by 512 columns by 8 bits wide. When the data bus interface to the DRAM side of the memory array is 16 bits wide, four 4-bit-wide 1 Meg VRAMs are required, each corresponding to one nibble of the 16-bit bus. A 16-bit data bus also exists on the SAM side.

When using 2 Meg VRAMs, only two devices are required (see Figure 2). The first corresponds to the byte formed by nibbles 0 and 1; the second, to nibbles 2 and 3. Similarly, on the SAM side, each pair of 512 x 4 SAMs (1 Meg VRAM) is replaced by a single 512 x 8 SAM (2 Meg VRAMs). Assuming that there is no need for NIBBLE READ accesses, this two-for-one replacement is transparent to the controller (NIBBLE WRITE accesses are available with the MT42C8254, if necessary, and will be covered under Feature Sets).

The examples depicted in figures 1 and 2 can be extended to wider controller-to-memory interfaces as well. (For example, in a 32-bit interface, four 2 Meg VRAMs would replace eight 1 Meg VRAMs.)

Example 2
Example 1 can also be extended to more than one bank of VRAMs simply by performing the two-for-one replacements within each bank. For example, a memory array configured as two banks of eight 1 Meg VRAMs would be replaced with two banks of four 2 Meg VRAMs (see Figures 3 and 4). In either case, the controller must include the necessary bank-select logic.

CASE 2: x8, 1 MEG VRAMs VS x8, 2 MEG VRAMs
Moving from 8-bit-wide 1 Meg VRAMs to 8-bit-wide 2 Meg VRAMs is somewhat more involved. This is shown in Examples 3 and 4.

Example 3
Figure 5 shows a 0.5 MB memory array based on 8-bit-wide 1 Meg VRAMs (Micron's MT42C8128). An equivalent memory array cannot be implemented with 2 Meg VRAMs due to the fact that four 2 Meg VRAMs are needed to form a 32-bit bus, and the resulting total memory array size then equals 1 MB. To move to 2 Meg VRAMs in this example requires a controller designed to support such memory expansion.

Example 4
On the other hand, a 1 MB memory array implemented with 8-bit-wide 1 Meg VRAMs would contain two banks (see Figure 6). Bank select logic determines which DRAMs and SAMs drive the respective busses at any given time.

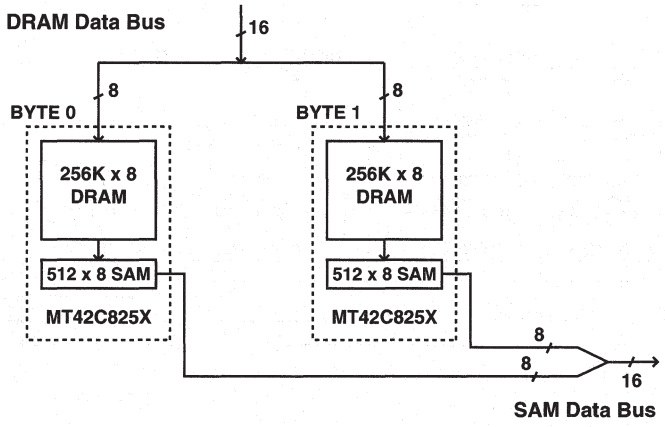


Figure 2
0.5 MB MEMORY ARRAY WITH A 16-BIT INTERFACE USING 2 MEG VRAMs

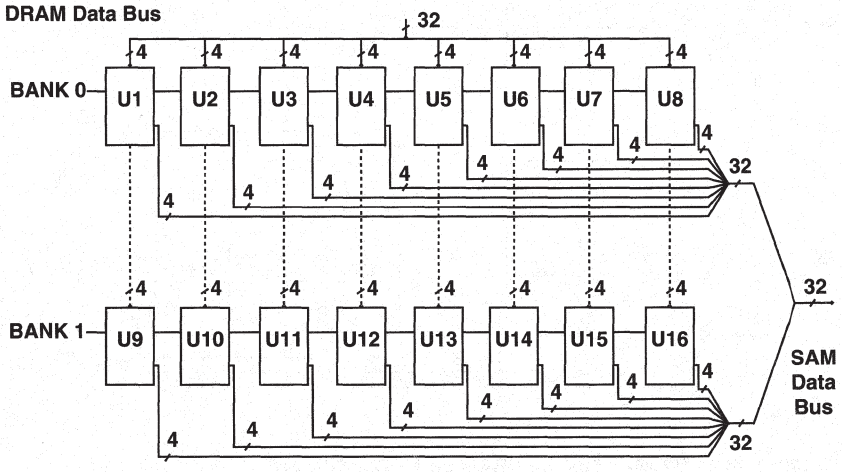
In this case, a memory array of equal size can be implemented with 2 Meg VRAMs; however, the array will consist of one bank instead of two (see Figure 7). This can be pictured as two-for-one replacements across the banks rather than within the banks. In this example, moving to 2 Meg VRAMs requires a controller that can address a second megabyte of memory through an additional column-address line rather than the bank-select logic used for the 1 Meg VRAM based implementation.

FEATURE SETS

When deciding upon the appropriate 2 Meg VRAM, there are three feature sets to consider. The first set is the one currently implemented in the 1 Meg VRAM-based design, the second and third sets are those offered by the two different categories of 2 Meg VRAMs. The first category, consisting of the Micron MT42C8254 and MT42C8255, provides standard features; the second, consisting of the MT42C8256 and MT42C8257, offers an extended feature set (see Table 1). In general, the standard features satisfy the requirements of PC graphics systems such as VGA/GUI accelerator designs, and the extended feature set addresses the needs of workstation graphics systems and communications systems.

When switching from 1 Meg VRAMs, designers will need to select an extended feature 2 Meg VRAM under any of the following conditions: 1) PERSISTENT WRITE functions were used at the 1 Meg level, 2) serial input or write transfers are required, 3) any of the functions introduced at the 2 Meg level will be supported. These additional features include the FLASH WRITE cycles, the MASKED WRITE TRANSFER cycles and the programmable split SAM. If an extended feature set 2 Meg VRAM is selected, the designer needs to be aware of some instruction decode changes between 1 Meg and 2 Meg VRAMs. Specifically, the input states which select a PERSISTENT MASKED WRITE to DRAM at the 1 Meg level are now used to select a MASKED FLASH WRITE to DRAM at the 2 Meg level. In order to support both features on one device, PERSISTENT WRITE functions are now selected automatically upon the loading of the mask register (and deselected with special $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ (CBR) cycles). Similarly, the input states that select an ALTERNATE WRITE TRANSFER at the 1 Meg level are now used to select a SPLIT WRITE TRANSFER at the 2 Meg level. The ALTERNATE WRITE TRANSFER is not offered at the 2 Meg level.

The above guidelines should be used to select the appropriate category of 2 Meg VRAMs. The next step is to determine which of the two devices within each category matches the needs of the specific application.



U1-U16: MT42C4256 VRAM (256K x 4 DRAM plus 512 x 4 SAM)

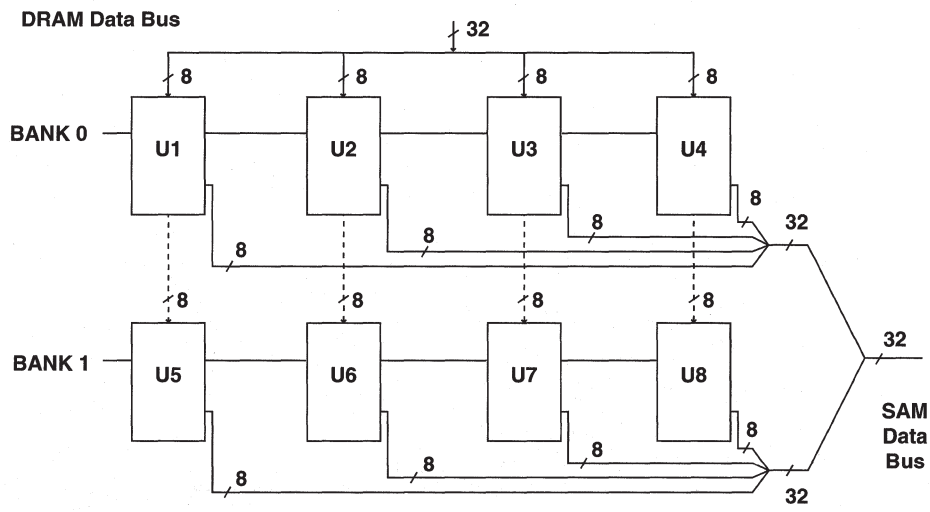
Figure 3
A 2 MB MEMORY ARRAY, WITH A 32-BIT INTERFACE, IMPLEMENTED WITH 1 MEG VRAMs

STANDARD FEATURE SET 2 MEG VRAMs: MT42C8254 VS MT42C8255

Once it is determined that a standard feature set 2 Meg VRAM is appropriate, the designer has a choice of either the MT42C8254 or the MT42C8255. The difference between the two is that the MT42C8254 provides a second WRITE ENABLE input in place of the QSF output. The second WRITE ENABLE provides NIBBLE WRITE capability. The QSF output available on the MT42C8255 indicates which half of the SAM is currently active (the half from which serial data is being read). The controller can use this information to initiate SPLIT READ TRANSFERS; however, many controllers keep track of this internally and do not require the QSF signal from the VRAM. If NIBBLE WRITE capability is required, the MT42C8254 must be used and the controller must monitor the SAM address internally. If NIBBLE WRITE capability is not required, the MT42C8255 is the appropriate choice.

EXTENDED FEATURE SET 2 MEG VRAMs: MT428256 VS MT42C8257

Similarly, once the need for an extended feature 2 Meg VRAM is established, the designer may choose either the MT42C8256 or the MT42C8257. The difference between these is that the MT42C8256 offers EXTENDED DATA-OUT on FAST-PAGE-MODE READ cycles, whereas the MT42C8257 offers standard FAST-PAGE-MODE operation. In FAST-PAGE-MODE operation with EXTENDED DATA-OUT, data being read out of the DRAM port is not disabled with the rising edge of $\overline{CAS}$ as it is in standard FAST-PAGE-MODE operation. This provides a psuedo-pipelined effect and achieves faster page mode cycle times. However, $\overline{OE}$ instead of $\overline{CAS}$ must be used to select banks in an interleaved configuration.



U1-U8: MT42C825X VRAM (256K x 8 DRAM plus 512 x 8 SAM)

Figure 4
A 2 MB MEMORY ARRAY, WITH A 32-BIT INTERFACE, IMPLEMENTED WITH 2 MEG VRAMs

PHYSICAL LAYOUT

There are no 2 Meg VRAM packages that are drop-in compatible with 1 Meg VRAM footprints. A board designed to accommodate both would have to include two sets of footprints, or a new board could be designed specifically for 2 Meg VRAM packages.

The 4-bit-wide 1 Meg VRAMs are offered in 28-lead ZIP or SOJ packages, while 2 Meg VRAMs are supplied in 40-lead SOJ or 40/44-lead TSOP packages. The 28 pins of the 1 Meg VRAM SOJ do not align with a subset of the 40 pins of the 2 Meg SOJ.

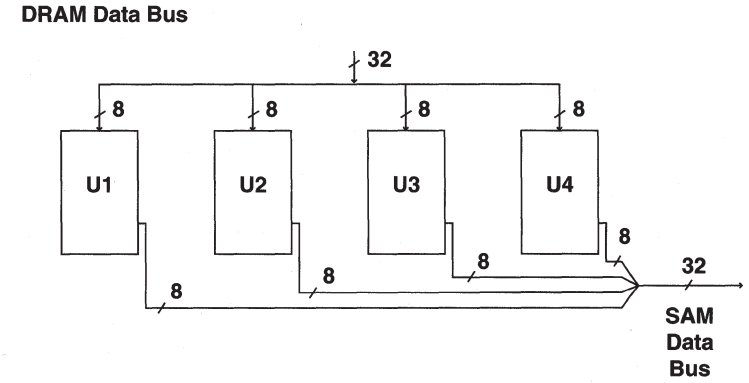
The 8-bit-wide 1 Meg VRAMs are available in 40-lead SOJ packages; however, the pin assignments do not align with those of the 2 Meg VRAM.

SUMMARY

Designers can increase system performance and reliability, while reducing board size and system costs by moving from 1 Meg VRAMs to 2 Meg VRAMs. The effort required to make this switch depends on memory configuration, required features, and physical layout. The effort might involve controller redesign, board layout redesign, or neither, if it was planned for in advance. In most cases, the added performance and reduced system costs will outweigh any forethought or redesign required.

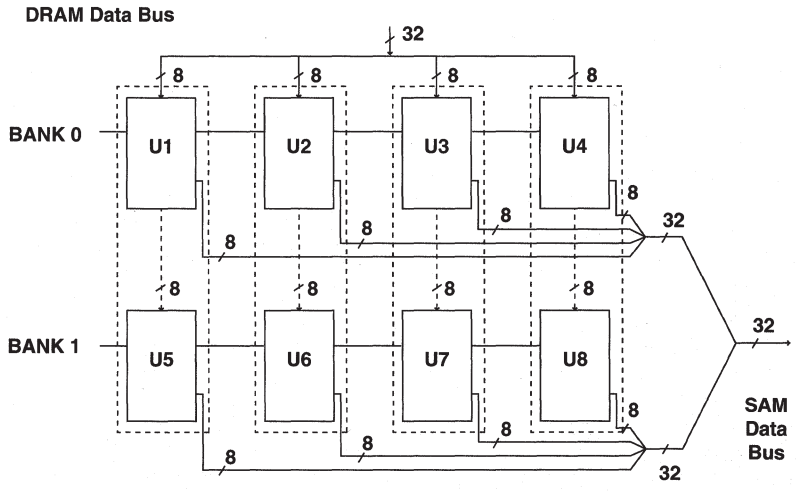
Table 1
FEATURE SETS OF 1 MEG AND 2 MEG VRAMs

Feature	1 Meg VRAM	2 Meg VRAM	
		Standard Set	Extended Set
DRAM OPERATIONS			
CBR REFRESH (RESET ALL OPTIONS)			■
CBR REFRESH (RESET STOP ADDRESS)			■
CBR REFRESH (NO RESET)	■	■	■
$\overline{\text{RAS}}$ ONLY REFRESH	■	■	■
NORMAL DRAM READ OR WRITE	■	■	■
NON PERSISTENT MASKED WRITE TO DRAM (NEW MASK)	■	■	■
PERSISTENT MASKED WRITE TO DRAM (OLD MASK)	■		■
BLOCK WRITE TO DRAM	■	■	■
NON-PERSISTENT MASKED BLOCK WRITE TO DRAM (NEW MASK)	■	■	■
PERSISTENT MASKED BLOCK WRITE TO DRAM (OLD MASK)	■		■
MASKED FLASH WRITE TO DRAM (NEW MASK)			■
MASKED FLASH WRITE TO DRAM (OLD MASK)			■
REGISTER OPERATIONS			
LOAD MASK REGISTER	■		■
LOAD COLOR REGISTER	■	■	■
TRANSFER OPERATIONS			
READ TRANSFER (DRAM-TO-SAM TRANSFER)	■	■	■
SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	■	■	■
WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NO MASK)	■		
PSEUDO WRITE TRANSFER	■		
ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	■		
MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER, NEW MASK)			■
MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER, OLD MASK)			■
MASKED SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER) (NEW MASK)			■
MASKED SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER) (OLD MASK)			■
PROGRAMMABLE SPLIT SAM			■



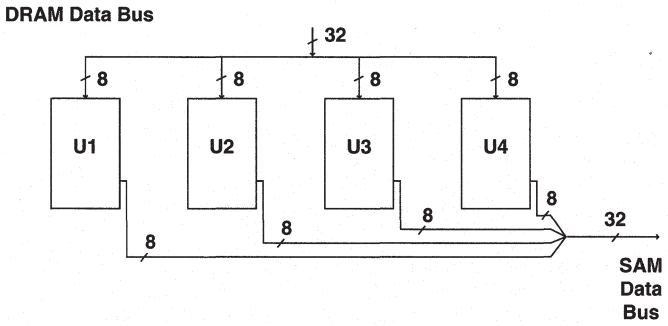
U1-U4: MT42C8128 VRAM (128K x 8 DRAM plus 256 x 8 SAM)

Figure 5
0.5 MB MEMORY ARRAY BASED ON 8-BIT-WIDE 1 MEG VRAMs



U1-U8: MT42C8128 VRAM (128K x 8 DRAM plus 256 x 8 SAM)

Figure 6
1 MB MEMORY ARRAY BASED ON 1 MEG VRAMs



U1-U4: MT42C825X VRAM (256K x 8 DRAM plus 512 x 8 SAM)

Figure 7
1 MB MEMORY ARRAY BASED ON 2 MEG VRAMs