OKI semiconductor

MSM41464

65,536-WORD x 4-BIT DYNAMIC RAM (PAGE MODE TYPE)

GENERAL DESCRIPTION

The Oki MSM41464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words x 4 bits. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address input permits MSM41464 housing in a standard 18 pin DIP or PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41464 offers new functional enhancements that make it more versatile than previous dynamic RAMs the $\overline{CAS}$-before-$\overline{RAS}$ refresh feature provides an on-chip refresh capability.

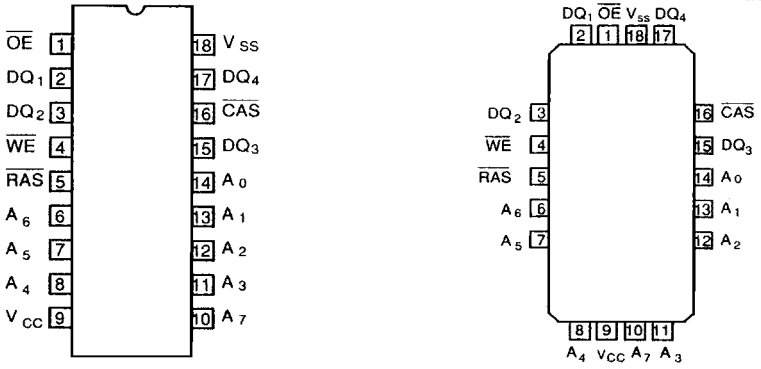
The MSM41464 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry, including the sense amplifiers, is employed in the design.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All input and output are TTL compatible.

FEATURES

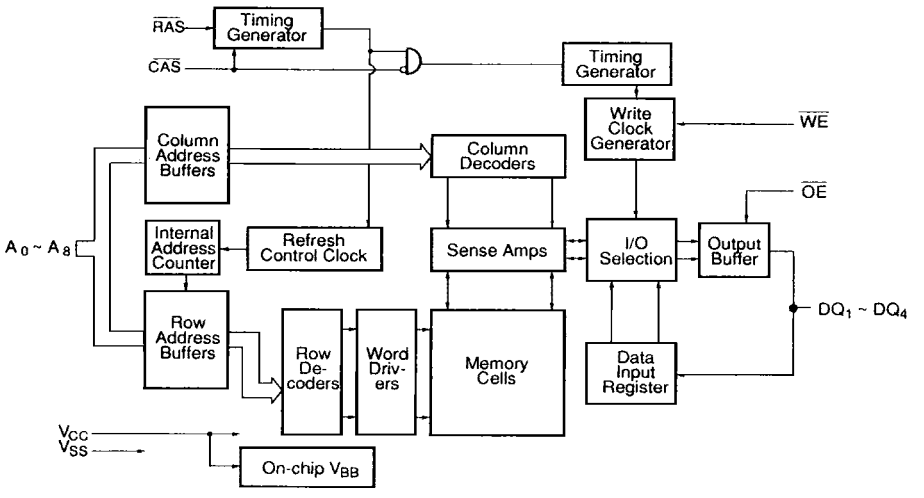
- 65,536 x 4 RAM, 18 pin package
- Silicon-gate, double poly NMOS, single transitor cell
- Row access time:
  - 100 ns max (MSM41464-10)
  - 120 ns max (MSM41464-12)
  - 150 ns max (MSM41464-15)
- Cycle time:
  - 200 ns min (MSM41464-10)
  - 220 ns min (MSM41464-12)
  - 260 ns min (MSM41464-15)
- Low power:
  - 385 mW active (MSM41464-10)
  - 360 mW active (MSM41464-12)
  - 330 mW active (MSM41464-15)
  - 28 mW max standby
- Single +5V power supply, ±10% tolerance
- TTL compatible, low capacitive load input
- Three-state TTL compatible output
- Gated $\overline{CAS}$
- 256 refresh cycles/4 ms
- Controllable output impedance through early write and $\overline{OE}$ operations
- Output unlatched at cycle end to allow extended page boundary and two-dimensional chip select
- Read-Modify-Write, and $\overline{RAS}$-only refresh capability
- On-chip latches for addresses and data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- Page Mode capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_7$	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$DQ_1 \sim DQ_4$	Data In / Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	–	–1 to +7	V
Operating temperature	T_{opr}	–	0 to 70	°C
Storage temperature	T_{stg}	–	–55 to +150	°C
Power dissipation	P_D	–	1.0	W
Short circuit output current	–	–	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Conditions	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	–	0	0	0	V	
Input high voltage, All Inputs	V_{IH}	–	2.4	–	6.5	V	
Input low voltage, All Inputs	V_{IL}	–	–1.0	–	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Conditions	MSM41464 Min.	MSM41464 Typ.	MSM41464 Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41464-10	I_{CC1}	–	–	–	70	mA	
	MSM41464-12					65		
	MSM41464-15					60		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	–	–	–	5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} ; t_{RC} = min.)	MSM41464-10	I_{CC3}	–	–	–	60	mA	
	MSM41464-12					55		
	MSM41464-15					50		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41464-10	I_{CC4}	–	–	–	45	mA	
	MSM41464-12					40		
	MSM41464-15					35		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41464-10	I_{CC5}	–	–	–	65	mA	
	MSM41464-12					60		
	MSM41464-15					55		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test =0V)		I_{LI}	–	–10	–	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	–	–10	–	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = –5 mA)		V_{OH}	–	2.4	–		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}				0.4	V	

* I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE *

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Value Min.	Value Max.	Unit
Input capacitance (A_0 ~ A_7)	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	7	pF
Data I/O capacitance (DQ_1 ~ DQ_4)	C_D	–	–	7	pF

* Capacitance measured width Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1,2,3

Parameter	Symbol	MSM41464-10		MSM41464-12		MSM41464-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	4	–	4	–	4	ms	–
Random read or write cycle time	t_{RC}	200	–	220	–	260	–	ns	–
Read-write cycle time	t_{RWC}	270	–	300	–	355	–	ns	–
Page mode cycle time	t_{PC}	100	–	120	–	145	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	4,5
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	4,5
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	–
Transition time	t_T	3	50	3	50	3	50	ns	–
$\overline{RAS}$ precharge time	t_{RP}	90	–	90	–	100	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	75	–	ns	–
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	60	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	70	10,000	ns	–
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	50	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	20	–	25	–	30	–	ns	–
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row address hold time	t_{RAH}	15	–	15	–	15	–	ns	–
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	–
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	7
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	6

AC CHARACTERISTICS (CONT.)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSM41464-10		MSM41464-12		MSM41464-15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write command pulse width	t_{WP}	25	–	30	–	35	–	ns	–
Write command hold time	t_{WCH}	25	–	30	–	35	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	35	–	40	–	45	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	35	–	40	–	45	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	–
Data-in hold time	t_{DH}	25	–	30	–	35	–	ns	–
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80	–	95	–	120	–	ns	6
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130	–	155	–	195	–	ns	6
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	20	–	ns	7
Access time from $\overline{OE}$	t_{OEA}	–	25	–	30	–	40	ns	–
$\overline{OE}$ data delay time	t_{OED}	25	–	30	–	40	–	ns	–
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	–
Turn-off delay time from $\overline{OE}$	t_{OEZ}	0	25	0	30	0	40	ns	–
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	30	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	20	–	25	–	30	–	ns	–
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	20	–	ns	–
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	30	–	ns	–
Read/write cycle (Refresh counter test)	t_{RTC}	380	–	430	–	510	–	ns	–
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	280	10,000	330	10,000	400	10,000	ns	–
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	70	–	ns	–
Read/write cycle time (Page mode)	t_{PRWC}	170	–	200	–	240	–	ns	–

Notes: 1. An initial pause of 100 μs is required after power-up followed by a minimum of any 8 $\overline{RAS}$ cycles (example: $\overline{RAS}$-only Refresh) before proper device operation is achieved.

2. The AC measurements assume the transition time (t_T) = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

4. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, the access time is controlled exclusively by t_{CAC}.

5. Measured using an equivalent load circuit of 2 TTL loads and 100pF.

6. The specs t_{WCS}, t_{RWD}, and t_{CWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an Early Write cycle and data out will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a Read-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out is indeterminate at access time.

7. Either the t_{RRH} or the t_{RCH} spec. must be satified for a proper read cycle.

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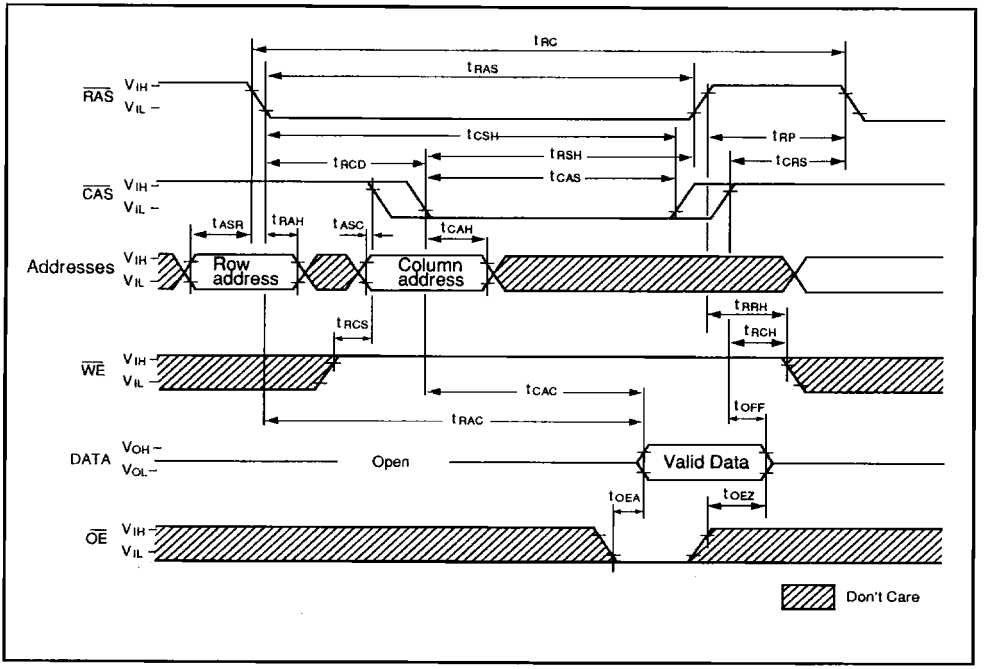
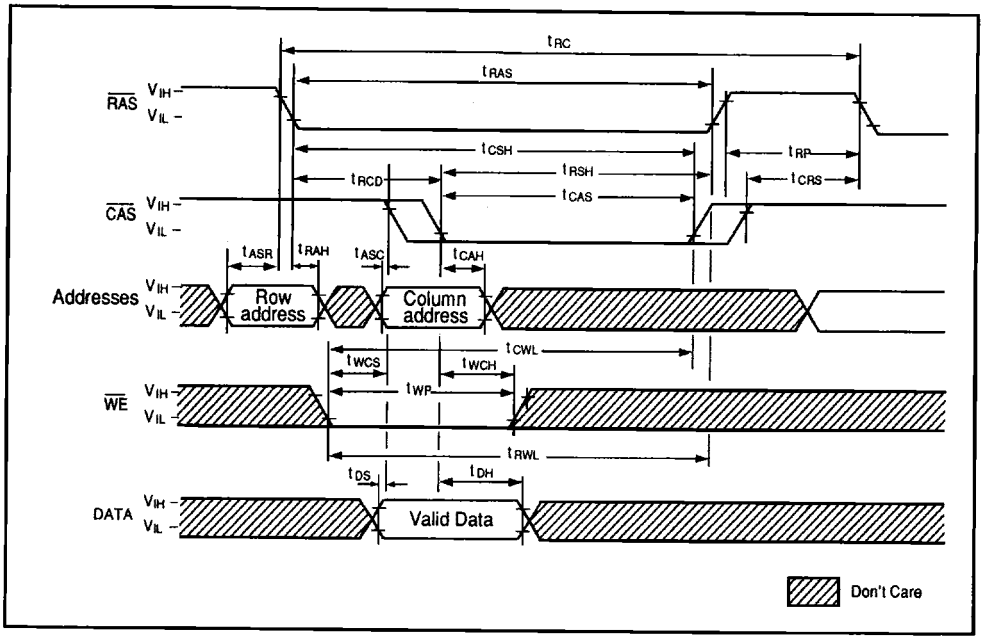
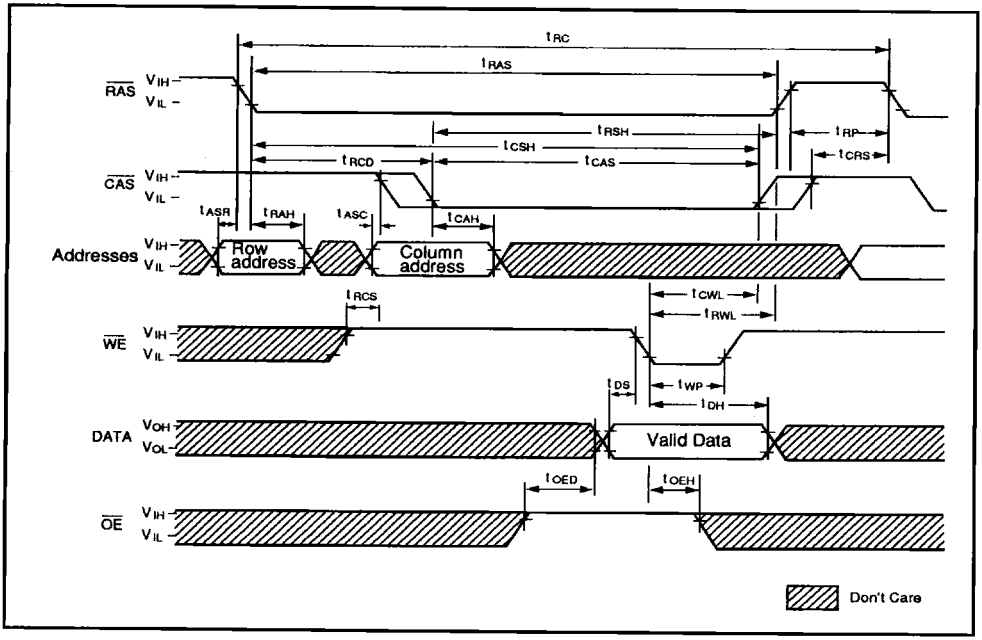
READ CYCLE



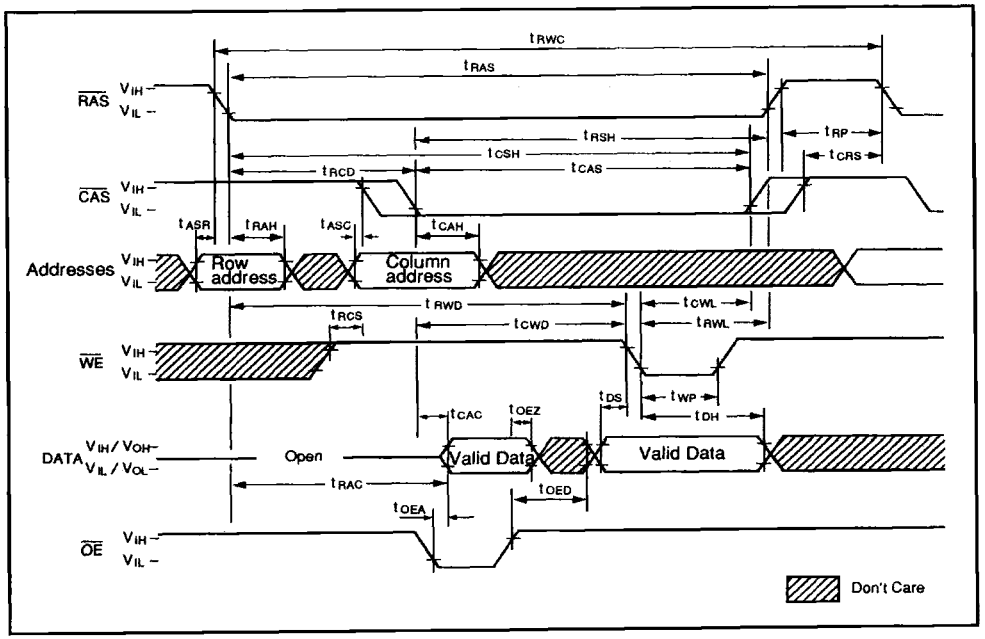
WRITE CYCLE (Early Write)



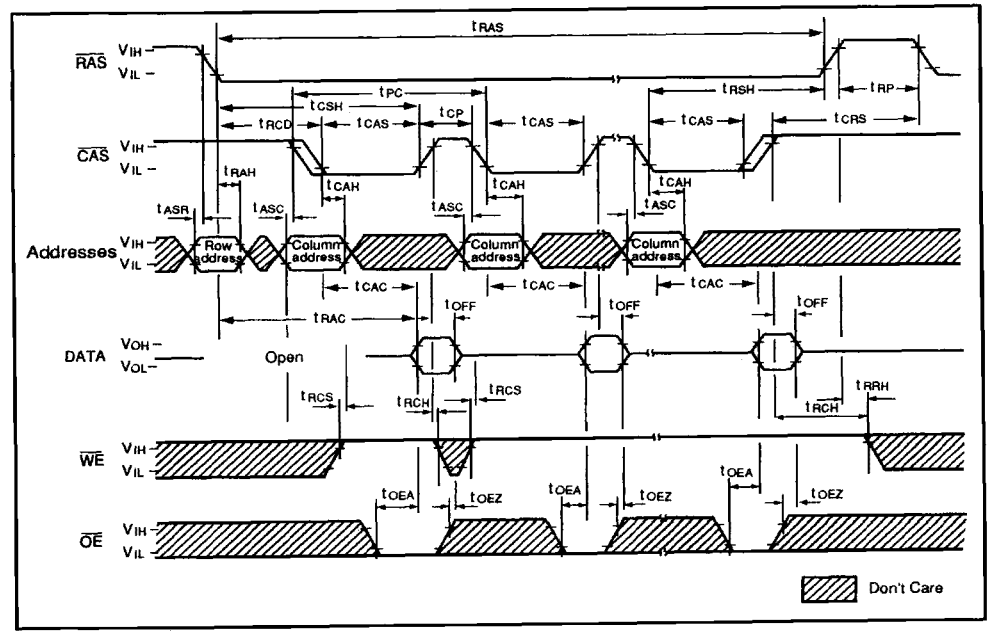
$\overline{OE}$ WRITE CYCLE



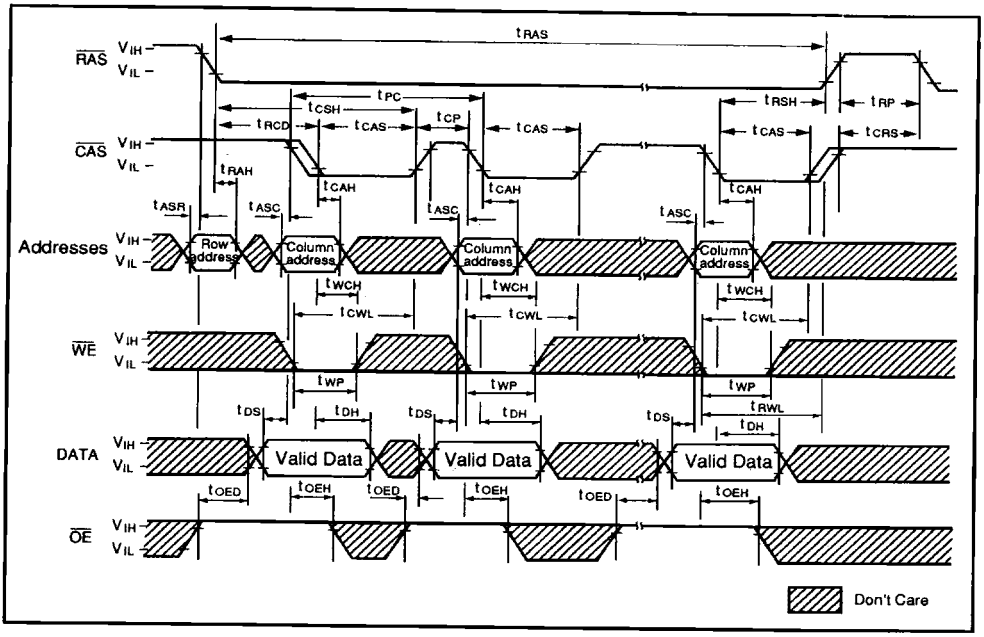
READ/WRITE AND READ MODIFY WRITE CYCLE



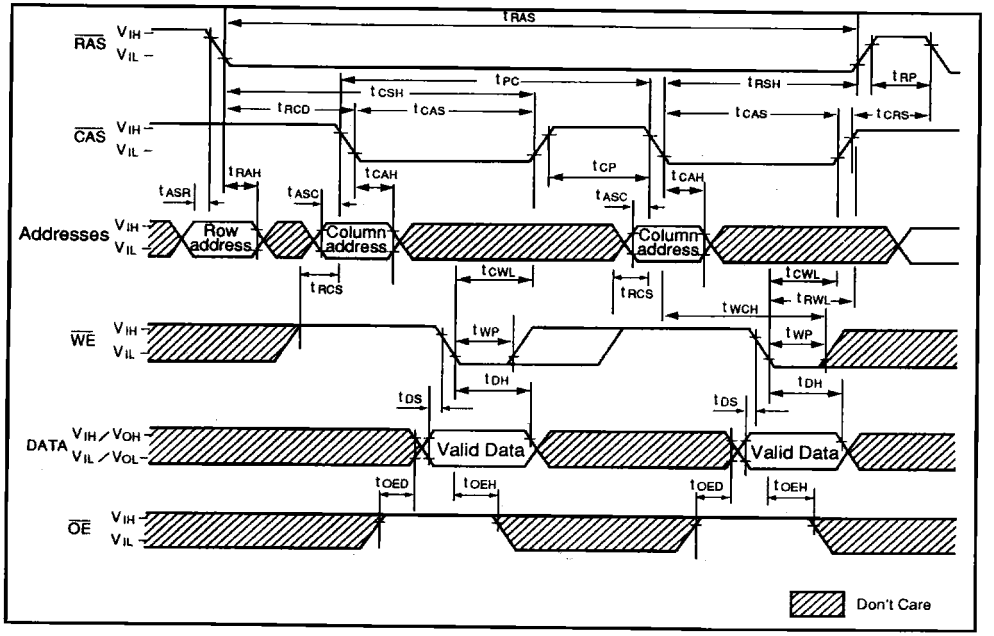
PAGE MODE READ CYCLE



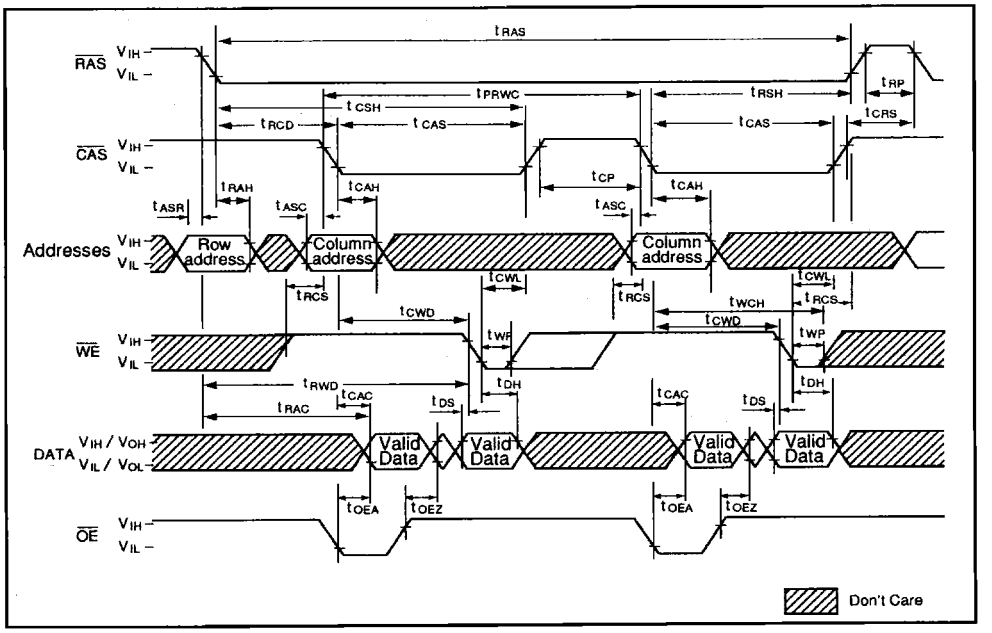
PAGE MODE WRITE CYCLE



PAGE MODE $\overline{OE}$ WRITE CYCLE



PAGE MODE READ/WRITE CYCLE



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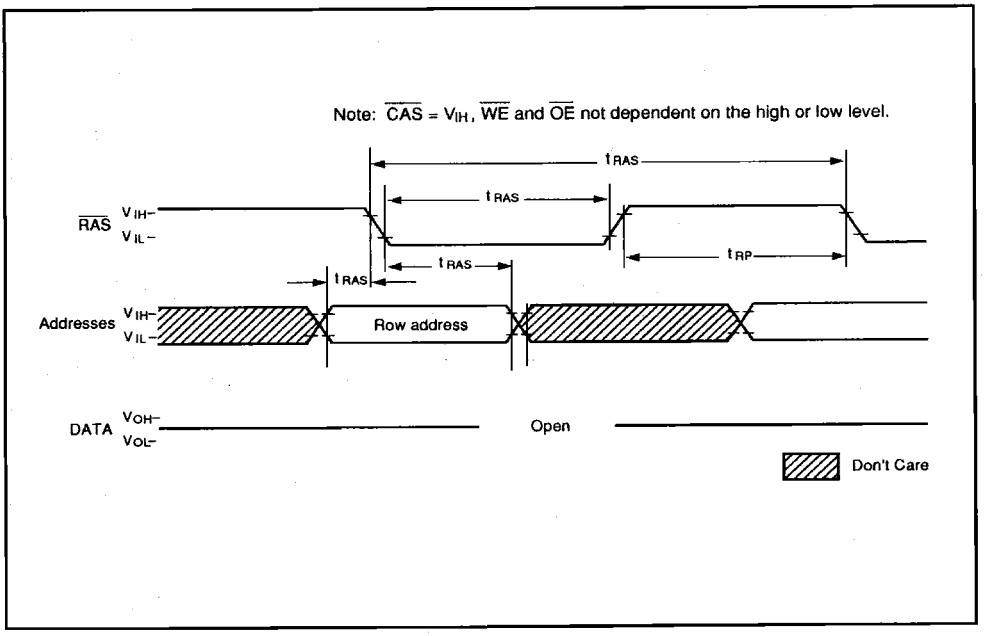
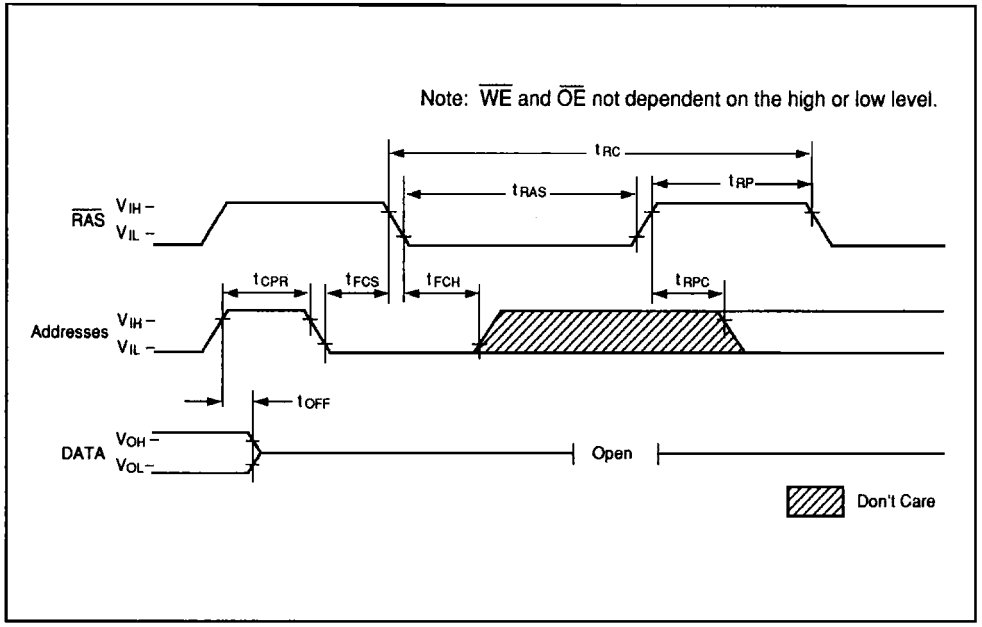
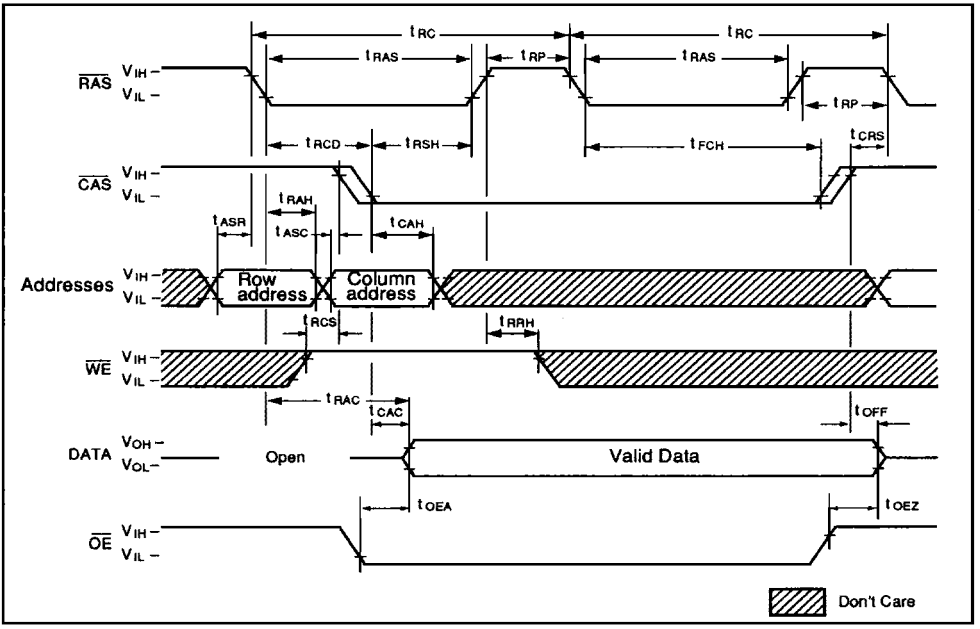
RAS-ONLY REFRESH CYCLE



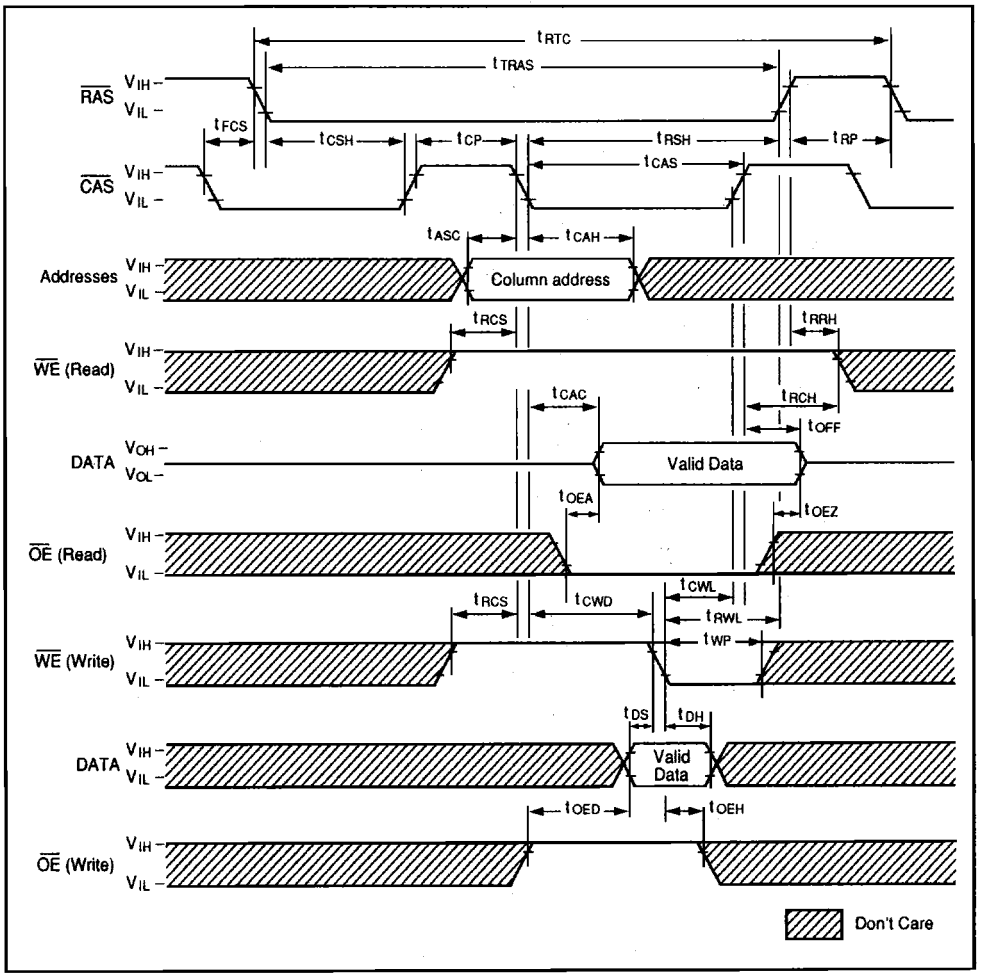
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



MSM41464 BIT MAP (PHYSICAL-DECIMAL)

DQ1 DQ2 DQ4 DQ3

☐ Pin 18

252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
130	130	130	130		130	130	130	130		130	130	130	130		130	130	130	130
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
130	130	130	130		130	130	130	130		130	130	130	130		130	130	130	130
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
253	253	253	253		253	253	253	253		253	253	253	253		253	253	253	253
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
253	253	253	253		253	253	253	253		253	253	253	253		253	253	253	253
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
125	125	125	125		125	125	125	125		125	125	125	125		125	125	125	125
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
125	125	125	125		125	125	125	125		130	130	130	130		125	125	125	125
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
2	2	2	2		2	2	2	2		2	2	2	2		2	2	2	2
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
2	2	2	2		2	2	2	2		2	2	2	2		2	2	2	2
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0
252	253	254	255		3	2	1	0		0	1	2	3		255	254	253	252
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0

COLUMN DECODER

REFRESH ADDRESS (0–255)

REFRESH ADDRESS (0–255)

☐ Pin 9

A / B :CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)