VIDEO PROCESSOR WITH DACs (VDA)

GENERAL DESCRIPTION

The SAA9060 is a video processor with DACs (VDA), which converts the digital luminance and chrominance data into analogue information for a RGB controller. The SAA9060 forms part of a chip-set for digital TV systems.

Features

- Single scan or double scan applications
- Parallel data input
- 7-bit D/A conversion of the colour difference signals
- 8-bit D/A conversion of the luminance signal

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Input current		I_{DD}	–	170	250	mA
Power dissipation		P_{tot}	–	–	1.4	W
Back-bias voltage			–3	–	0	V
Operating ambient temperature range		T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

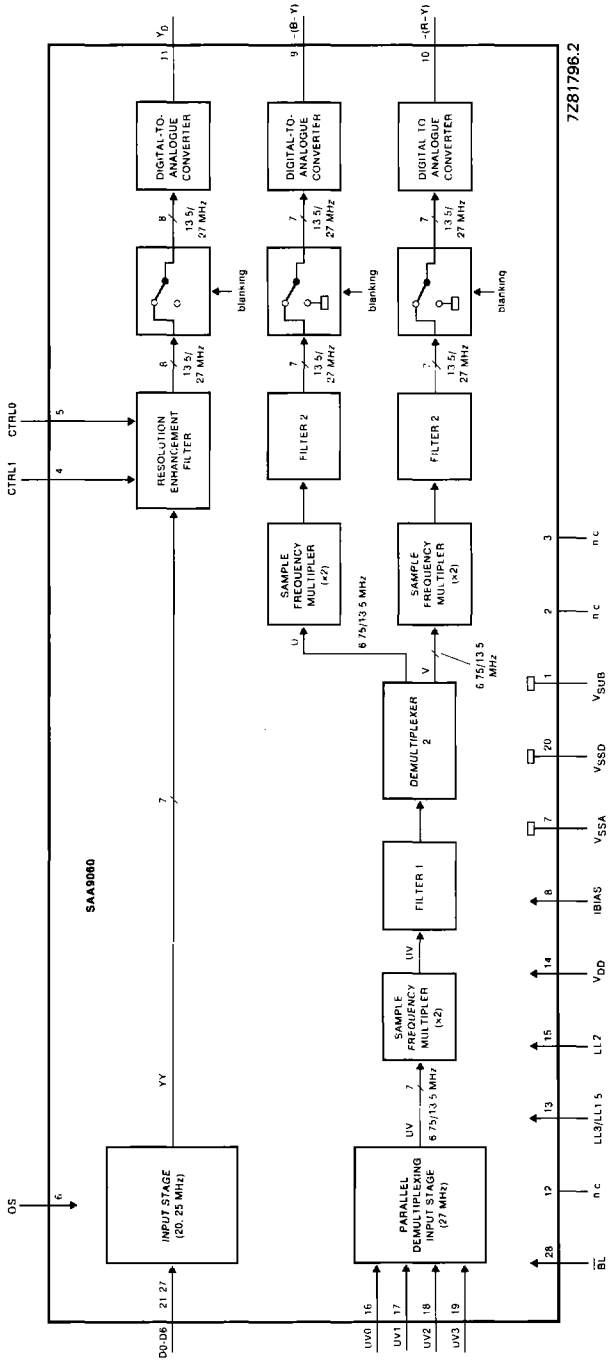


Fig.1 Block diagram.

PINNING

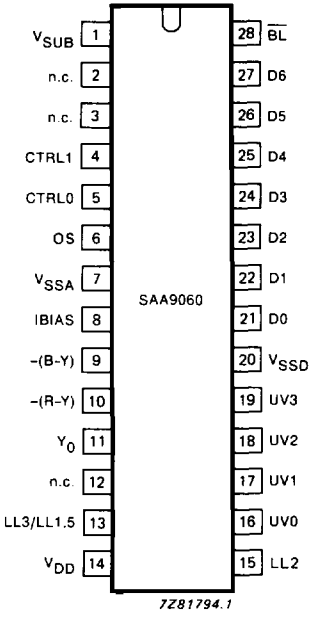


Fig.2 Pinning diagram.

1	V_{SUB}	Substrate pin for external capacitor, smooths internally generated voltages
2, 3	n.c.	Not connected
4	CTRL1	Control input for resolution enhancement filter
5	CTRL0	Control input for resolution enhancement filter
6	OS	Data format switch-over (from serial to parallel) at inputs DO...D6, UVO...UV3, BLN
7	V_{SSA}	Analogue ground
8	IBIAS	Reference current for the DACs
9	–(B-Y)	Chrominance analogue output; inverted colour difference signal B-Y
10	–(R-Y)	Chrominance analogue output; inverted colour difference signal R-Y
11	Y_O	Luminance analogue output
12	n.c.	Not connected
13	LL3/ LL1.5	Clock input: single scan parallel mode, f = 13.5 MHz double scan parallel mode, f = 27 MHz

PINNING (continued)

14	V_{DD}	Supply voltage
15	LL2	(Clock input for data word D0...D6) for serial data format only*/ f = 20.25 MHz; low-level version Do not connect pin when selecting parallel data format
16	UV0	Digital chrominance input; f = 13.5 MHz or 27 MHz
17	UV1	
18	UV2	
19	UV3	
20	V_{SSD}	Digital ground (0 V)
21	D0	Digital 7-bit luminance input; f = 13.5 MHz or 27 MHz
22	D1	
23	D2	
24	D3	
25	D4	
26	D5	
27	D6	
28	$\overline{BL}$	Format input; indicates the start of a transmission of a data line

FUNCTIONAL DESCRIPTION (see Fig. 1)

The VDA, DMSD/S-DMSD and a RGB controller form the video channel of a digital TV system. The VDA receives the luminance and chrominance data from the DMSD/S-DMSD and converts this data into an analogue output for a RGB controller.

Chrominance data signal

The chrominance data consist of alternating UV samples with a sample frequency of 3.375 MHz (single scan), the sample frequency is increased to 13.5 MHz by using two cascaded interpolation filters. The 7-bit chrominance data is then converted to an analogue signal (inverted colour difference signals B-Y and R-Y) for use in a RGB controller.

Luminance data signal

The luminance data frequency is clocked at 13.5 MHz or 27 MHz into the resolution enhancement filter (controlled by CTRL0 and CTRL1), this improves the quantization noise behaviour in areas with small variation and produces an 8-bit data output. The 8-bit data is converted into an analogue signal for use in a RGB controller.

$\overline{BL}$ signal (see Fig. 3)

The $\overline{BL}$ signal is used to indicate the active video length within the line and synchronizes the demultiplexing of the UV data.

Operating modes

There are two operating modes:

- parallel data transmission (single scan); LL3/LL1.5 = 13.5 MHz
- parallel data transmission (double scan), LL3/LL1.5 = 27 MHz.

Output signals

The output signals are AC-coupled to a RGB controller. During the horizontal synchronization gap the luminance and chrominance signals are blanked (black and no colour difference respectively) and the RGB controller clamps the input signals.

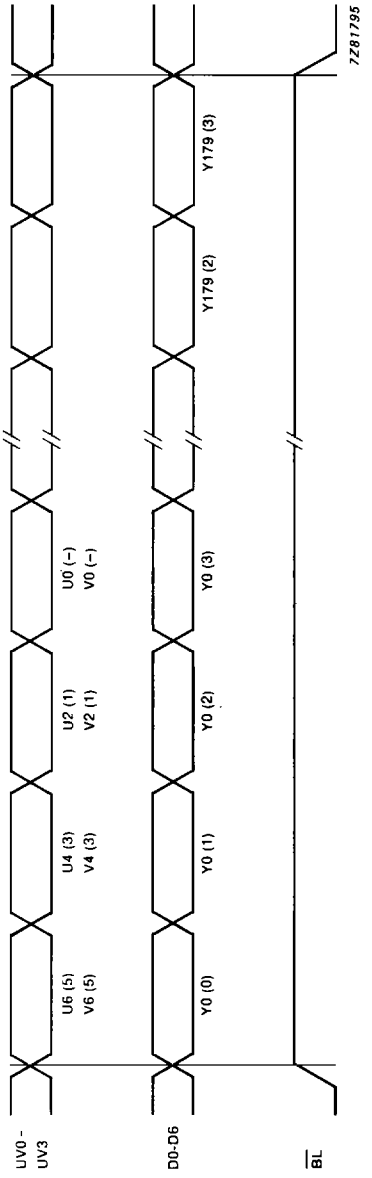


Fig.3 Data format.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.3	6.0	V
Input voltage		V_I	−0.5	6.0	V
Back-bias voltage		V_{BIAS}	−3	0	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

Junction to ambient	$R_{th\,j\text{-}a}$	50 K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all values referred to V_{SS}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	*	170	250	mA
Voltage on pin 1	with clock	V_{SUB}	−3.0	−2.5	−2.0	V
Current on pin 1	without clock	I_{SUB}	−	0.2	40	μA
Voltage ripple on pin 1		V_{ripple}	−	−	10	mV
Inputs						
LL3 input signal	note 1; see Fig. 4					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL3 time period	f_{nom} = 13.5 MHz	t_{LL3}	69	74	80	ns
Duty factor		t_{PH}/t_{LL3}	43	50	57	%
LL1.5 input signal	note 2; see Fig. 5					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL1.5 time period	f_{nom} = 27 MHz	$t_{LL1.5}$	35	37	40	ns
Duty factor		$t_{PH}/t_{LL1.5}$	43	50	57	%

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{BL}$ input signal	note 3; see Figs 6 and 7					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
Pulse width HIGH		t_{PH}	–	720	–	*
Pulse width LOW	NTSC/PAL	t_{PL}	–	138/144	–	*
LL3 set-up time		t_{SU}	12	–	–	ns
D0-D6 and UV0 to UV3	note 2; see Fig. 8					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
LL1.5 set-up time		t_{SU}	13	–	–	ns
LL1.5 hold time		t_{HD}	3	–	–	ns
CTRL0 and CTRL1 input signals	note 4					
Input voltage HIGH	note 5	V_{IH}	2	–	V_{DD}	V
Input voltage LOW	note 5	V_{IL}	V_{SS}	–	0.8	V
Input capacitance**	V_I = 0 V	C_I	–	–	10	pF
IBIAS input signal	Fig. 9					
Input current	note 6	I_{IBIAS}	–	100	–	μA
Bias resistance	note 7	R_{IBIAS}	–	39	–	kΩ
Input voltage	note 7	V_{IBIAS}	–	V_{DD}	–	V
Potential difference across R_{IBIAS}	note 8	U_{IBIAS}	–	1.5	–	V

* Clock periods of LL3.
** Referred to pin 20.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
Y signal output	note 9					
Resolution			–	8	–	bits
Nominal range	max. 255		14	–	230	
Output current	max. 2.55	I_O	0.14	–	2.3	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	10	–	μA
Load on pin 11		R_L	–	180	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	47	–	nF
Total output capacitance (pin 11)	note 10	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS} = 0$		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB
−(B-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		13	–	114	
Output current		I_O	0.26	–	2.28	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 9		R_L	–	750	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 9)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS}=0$		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB
−(R-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		10	–	117	
Output current	max. 2.55		0.2	–	2.34	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 10		R_L	–	560	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 10)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	ΔI_{IBIAS}		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB

IENT DATA

Notes to the characteristics

1. 25/30 Hz picture frequency with interlace.
2. 50/60 Hz picture frequency, parallel data transmission.
3. 25/30 Hz picture frequency, f = 20.25 MHz.
4. Static input signal; input HIGH by means of an internal pull-up resistor of 100 kΩ.
5.

CTRL1	CTRL0	filter function
0	0	bypass (min.)
1	1	lowpass (max.)

6. When I_{IBIAS} = 100 μA the quantization steps of the Y output DAC is 10 μA and −(B-Y), −(R-Y) outputs are 20 μA. The maximum voltage at R_L is 2 V. If R_{IBIAS} is used, the temperature coefficients of I_{BIAS} and the DACs are compensated.
7. Effective voltage noise is ⩽ 1 mV.
8. $U_{IBIAS} = 1.2\ V + I_{IBIAS} \times 3\ k\Omega$.
9. Values measured from the Y output DAC.
10. Values measured from the −(B-Y) output DAC.

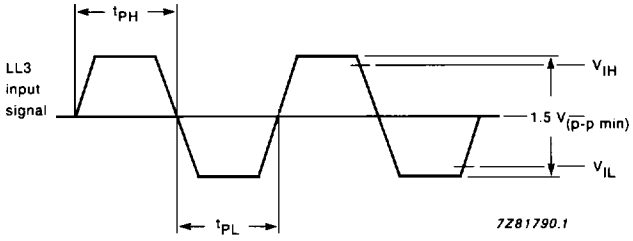


Fig. 4 LL3 timing waveform; 25/30 Hz picture frequency with interlace.

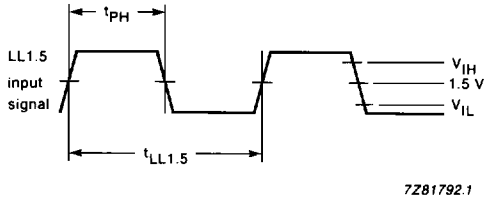


Fig. 5 LL1.5 timing waveform; 50/60 Hz picture frequency, parallel data transmission.

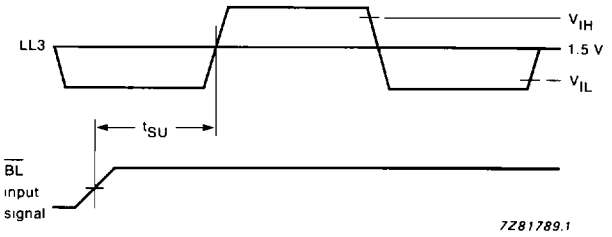


Fig. 6 $\overline{BL}$ timing waveform; 25/30 Hz picture frequency; f = 13.5 MHz.

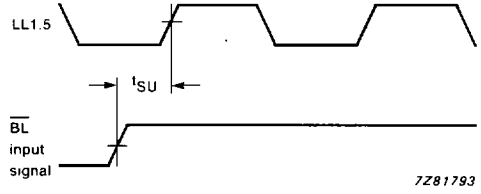


Fig. 7 $\overline{BL}$ timing waveform; 50/60 Hz picture frequency; f = 27 MHz.

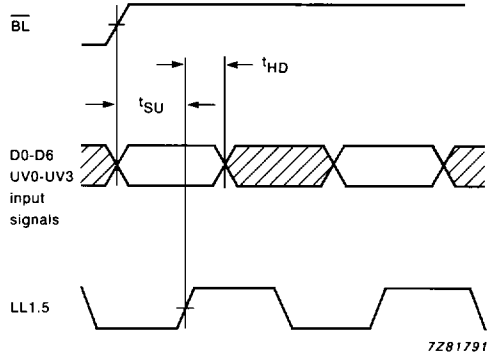


Fig. 8 D0 to D6 and UV0 to UV3 timing waveform; 50/60 Hz picture frequency, f = 27 MHz.

APPLICATION INFORMATION

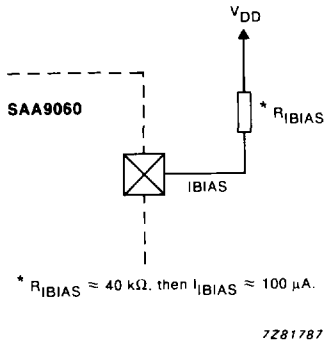
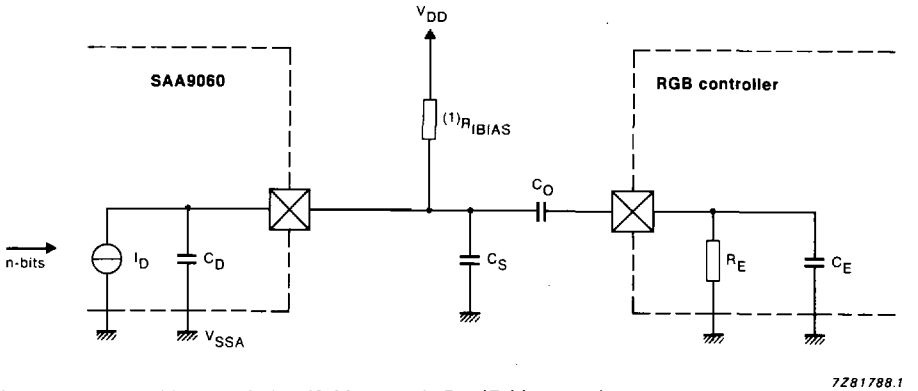


Fig. 9 IBIAS input circuit.



(1) $R_{IBIAS} = R_L$ (Y output), R_L (B-Y output), R_L (R-Y output)

Fig. 10 Application of the DACs.